

PG142-B00

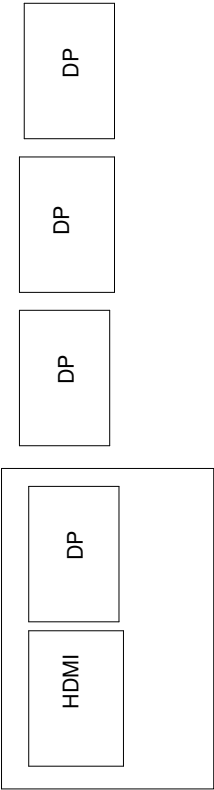
DP + DP + DP + HDMI/DP

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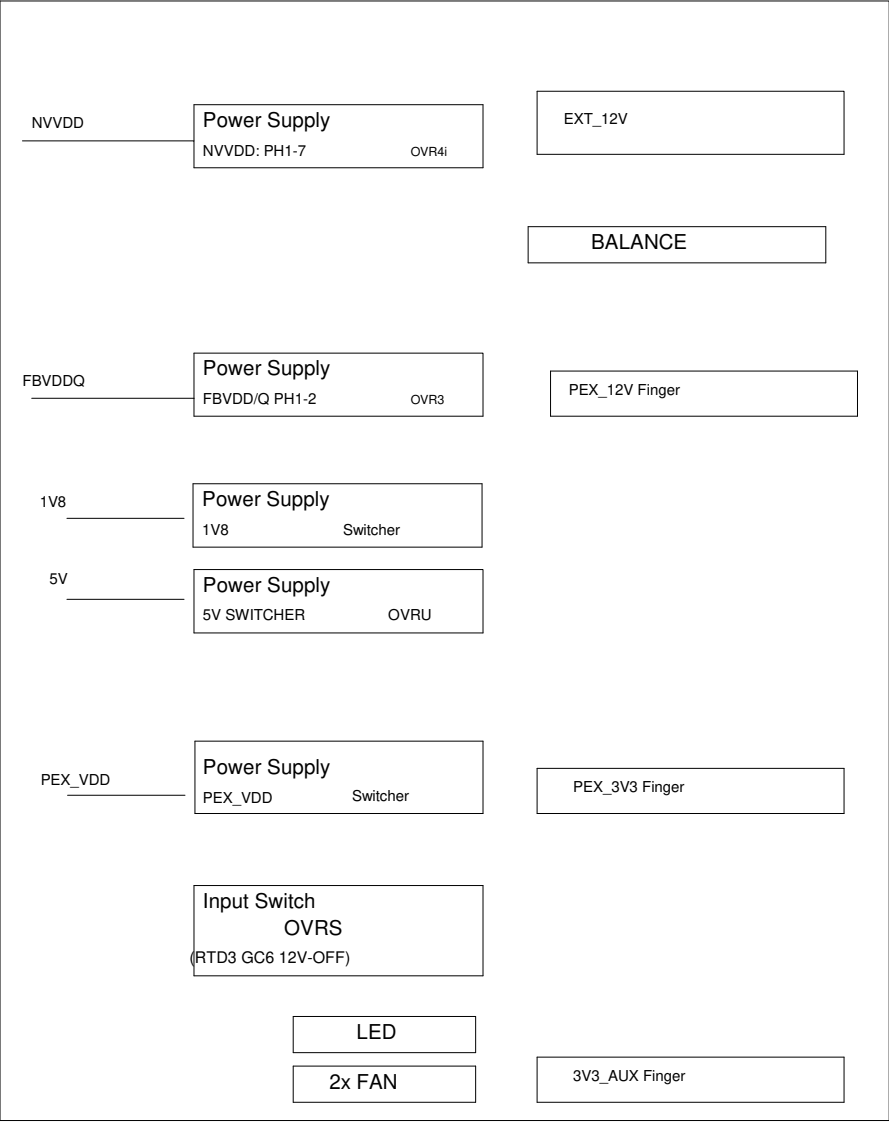
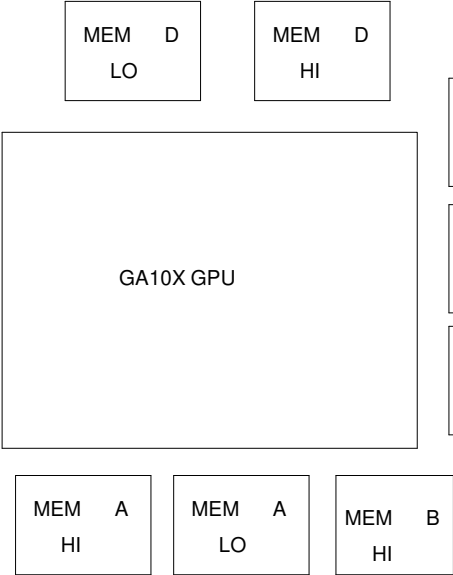
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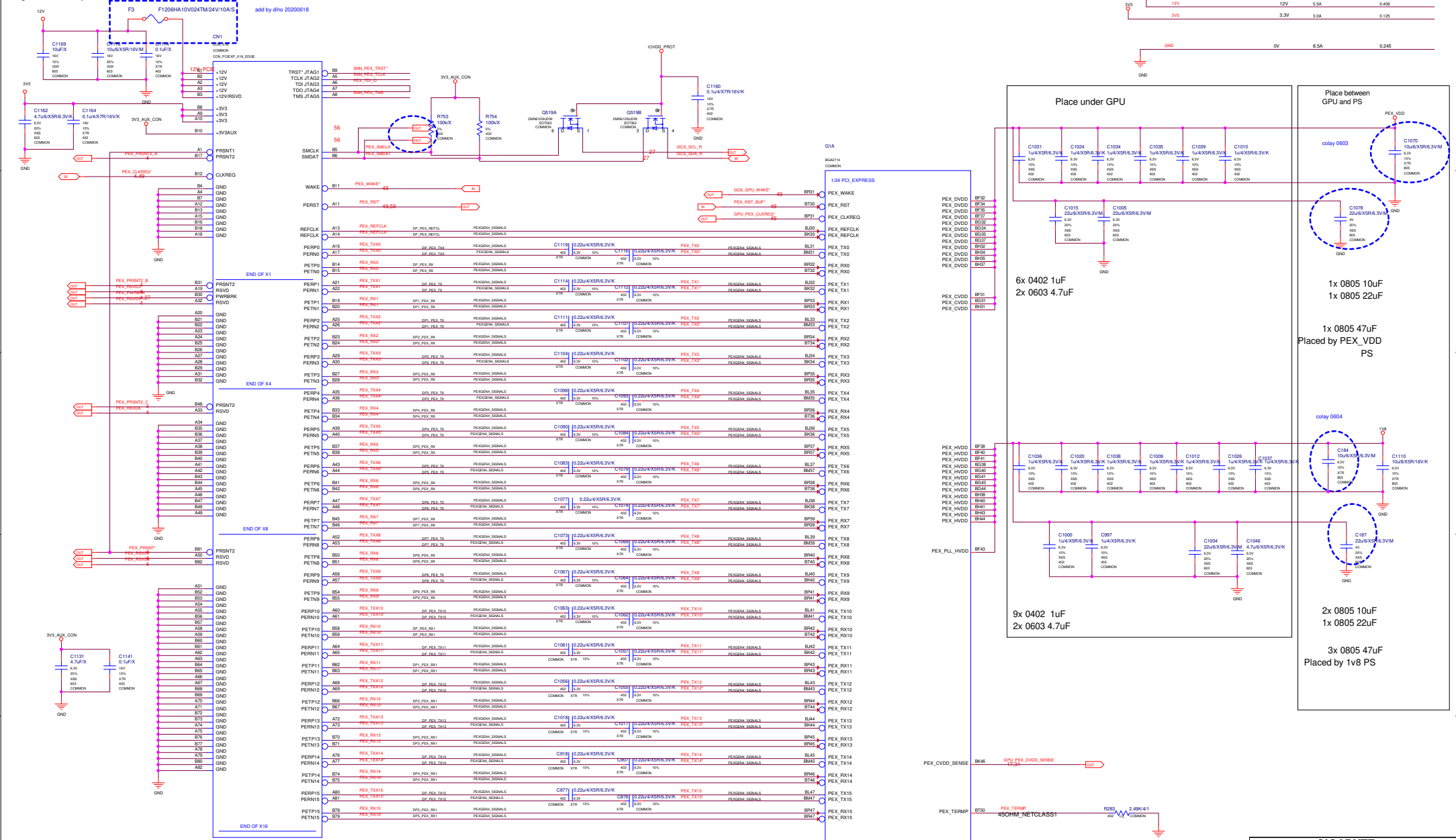
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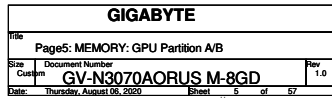


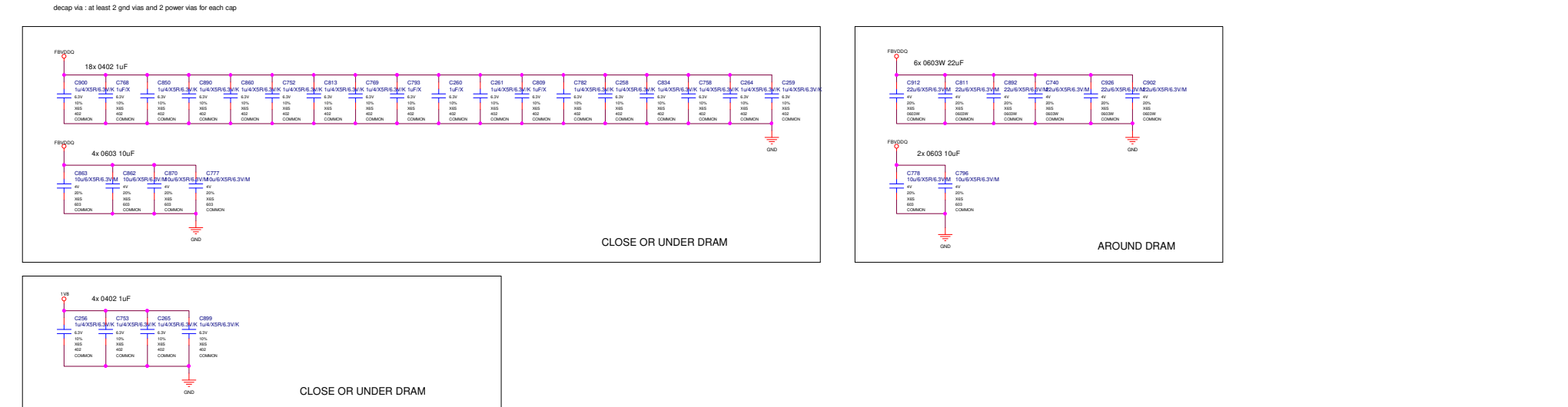
POWER SUPPLY

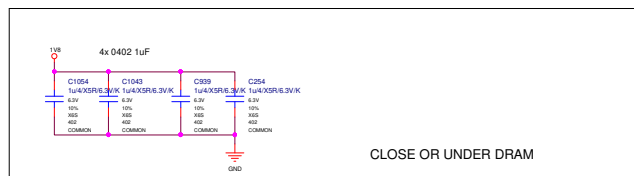
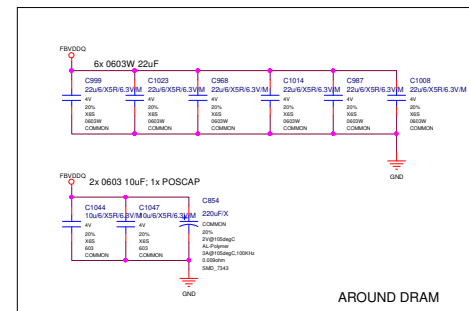
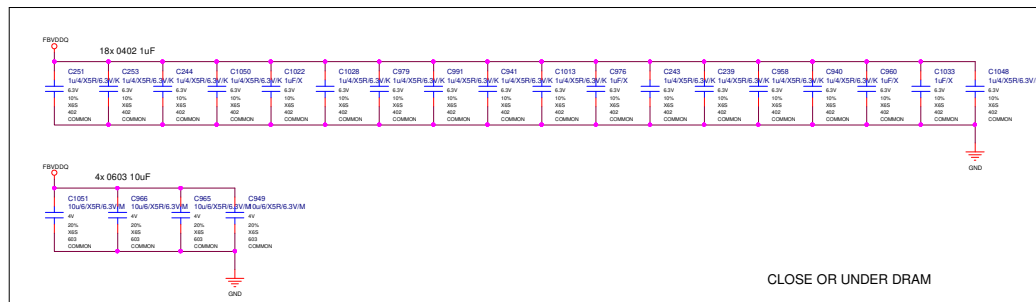
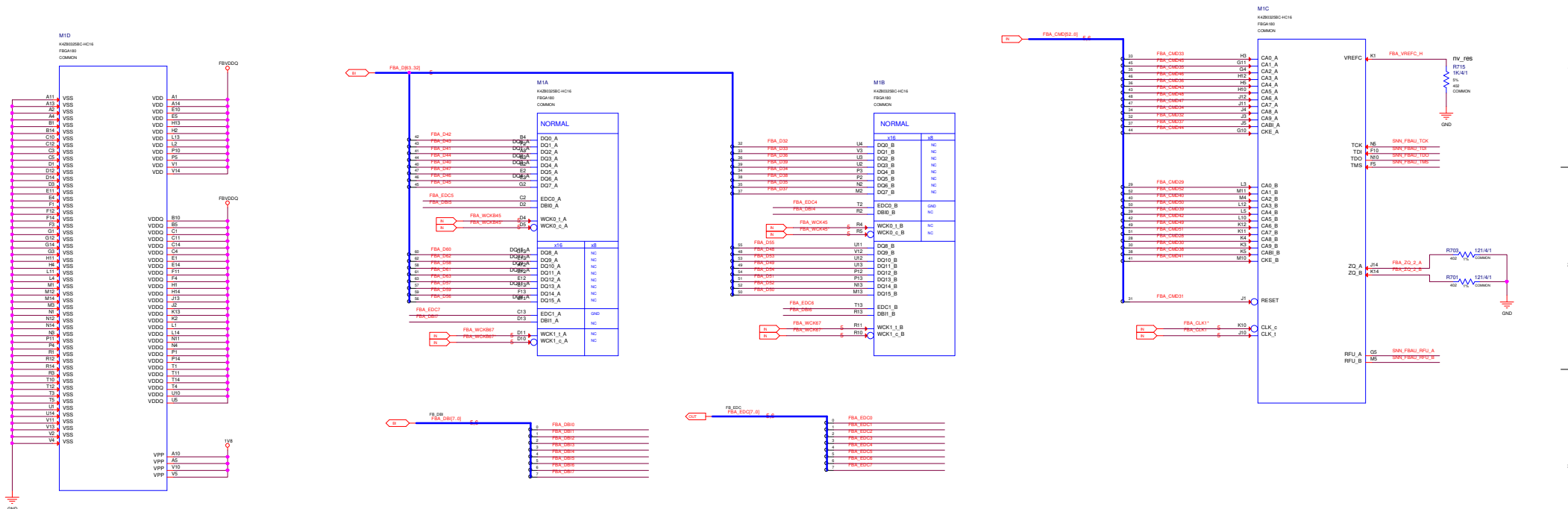


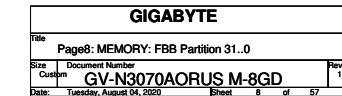
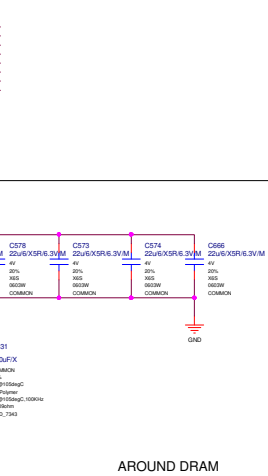
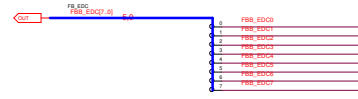
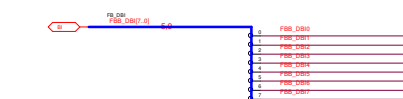
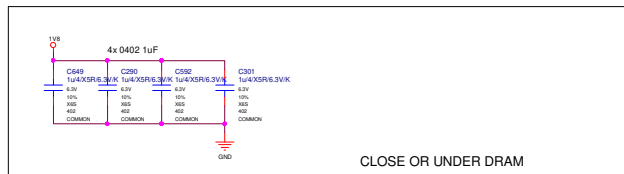




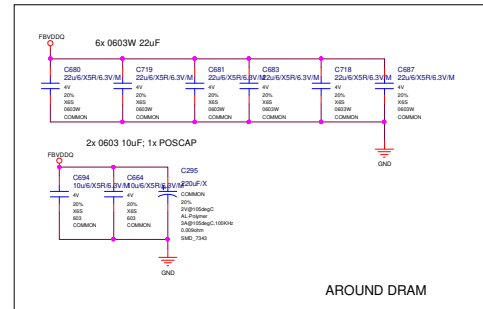
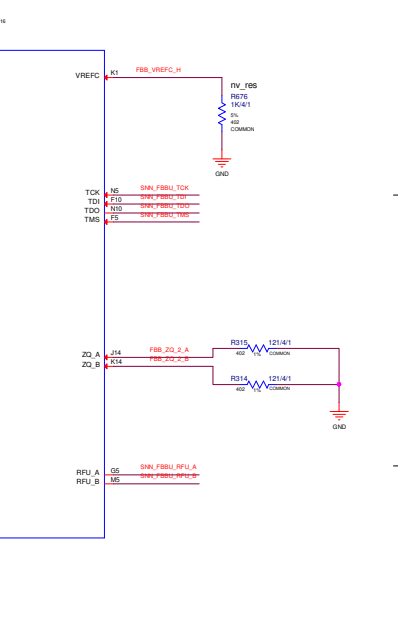




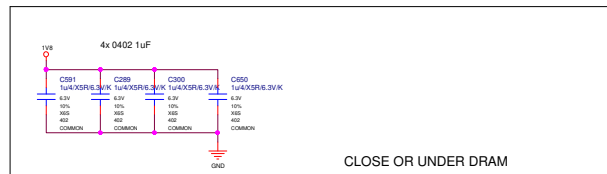


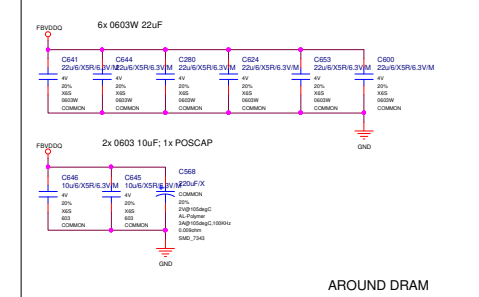
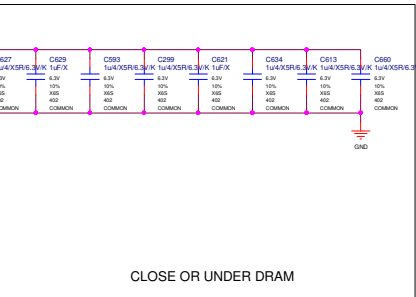
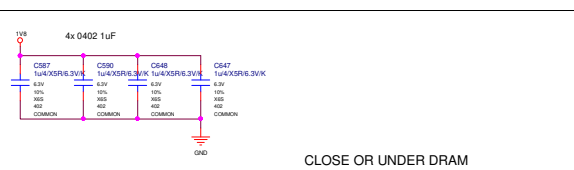


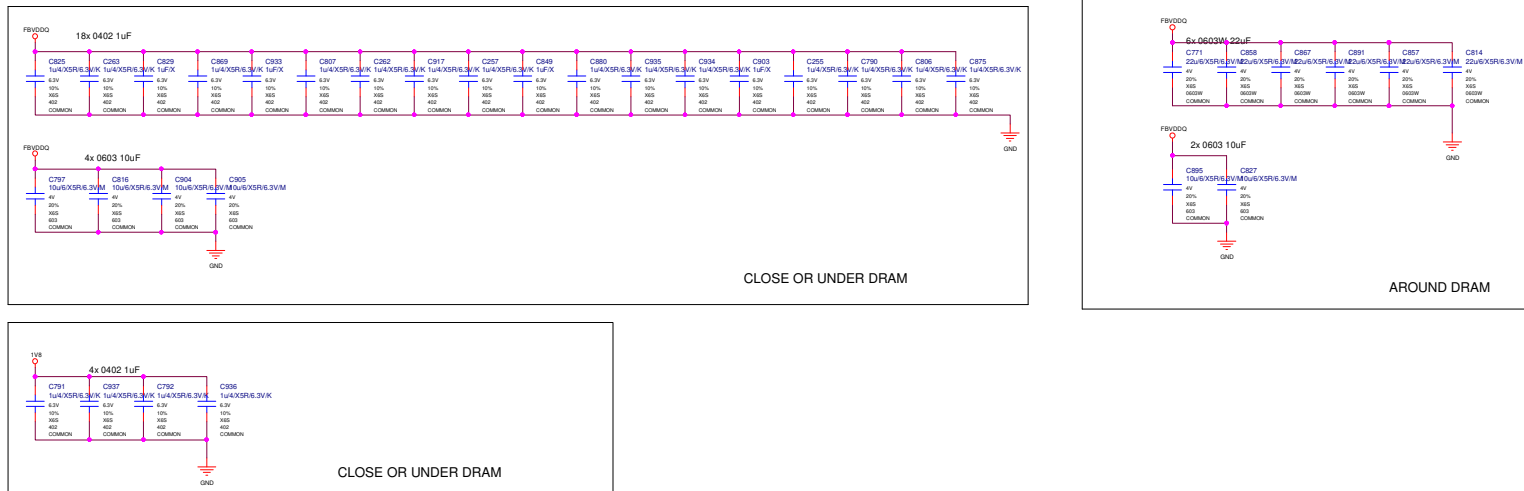


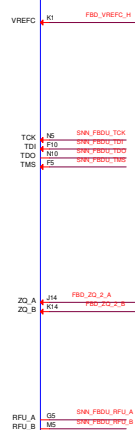
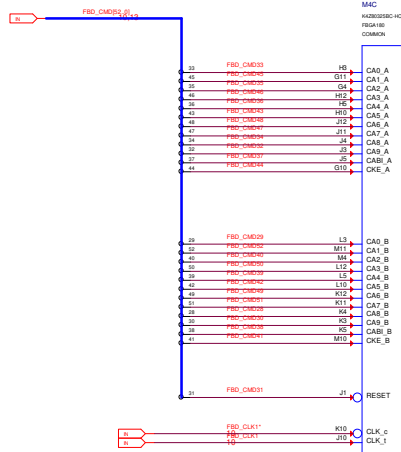
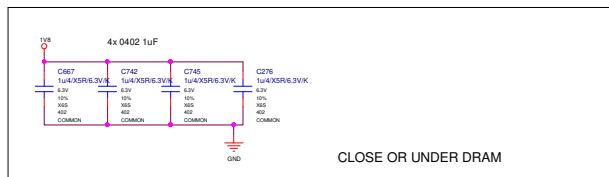
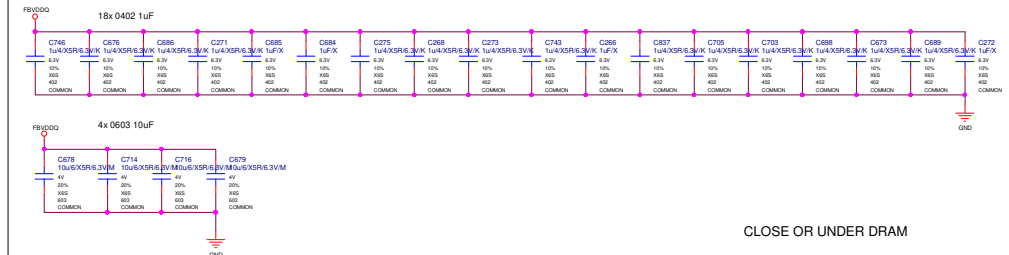
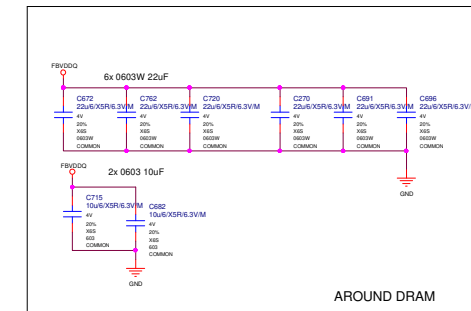
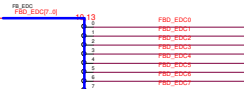
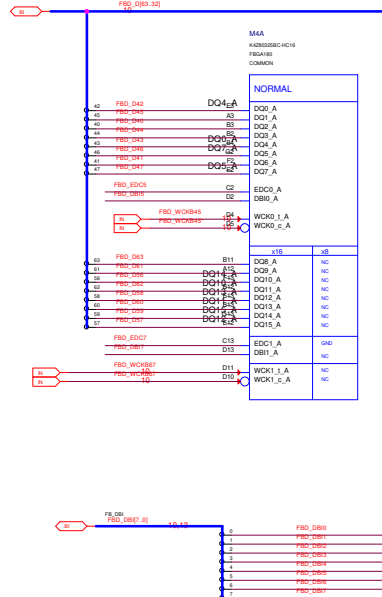




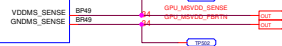




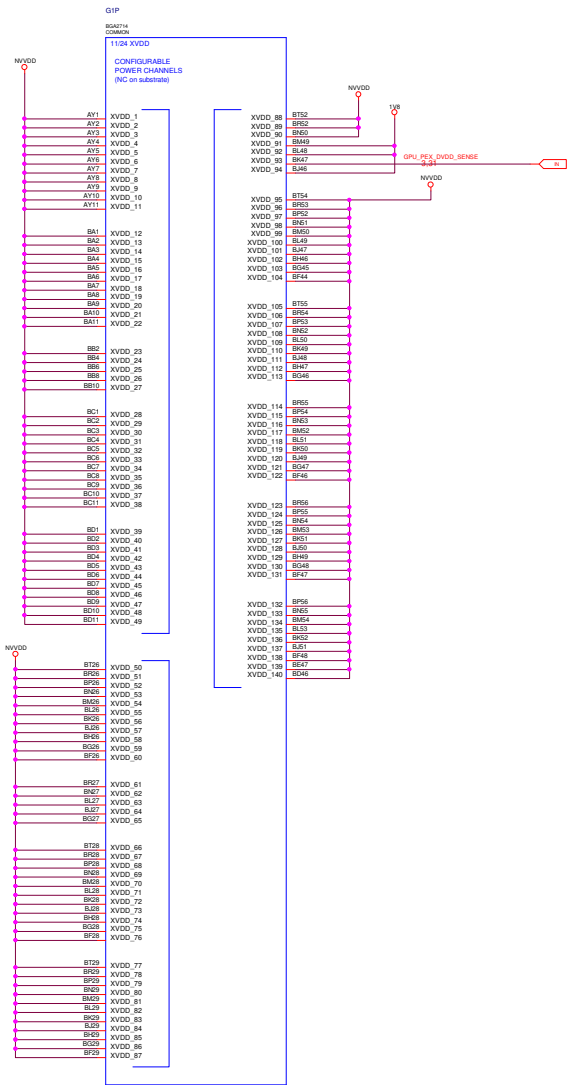




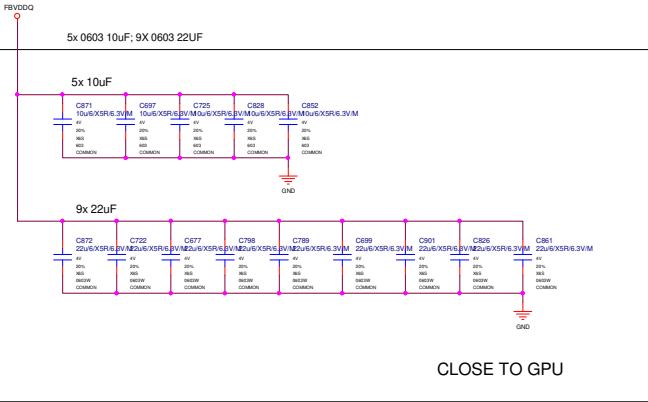
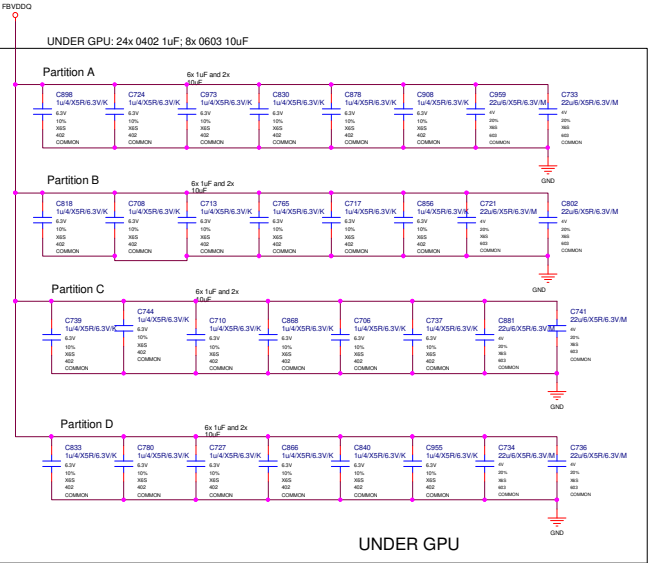


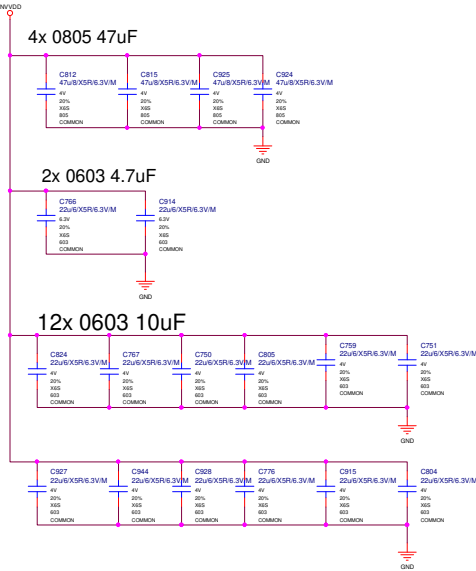
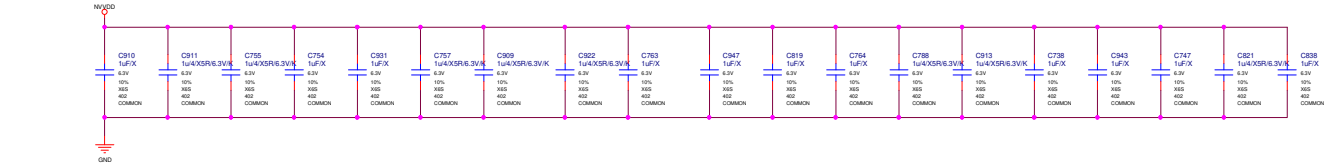
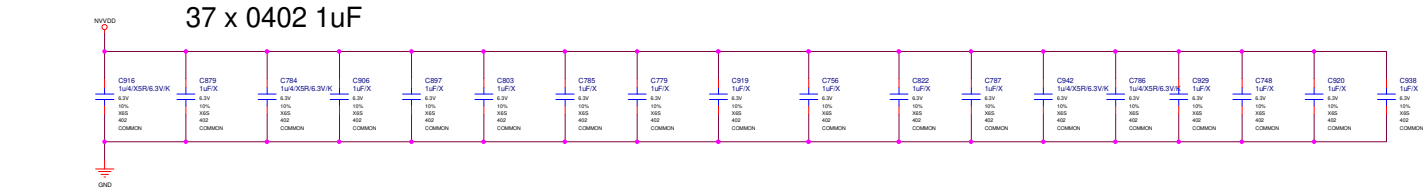
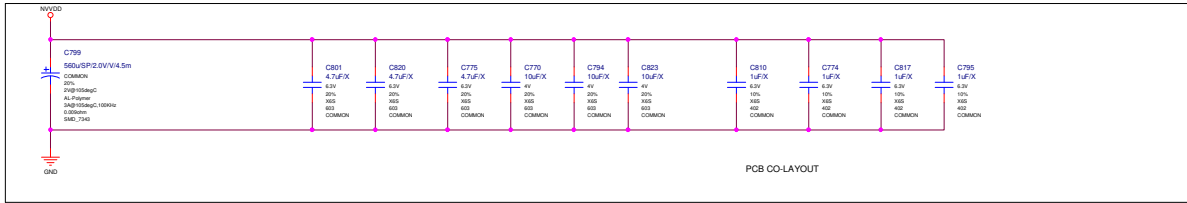
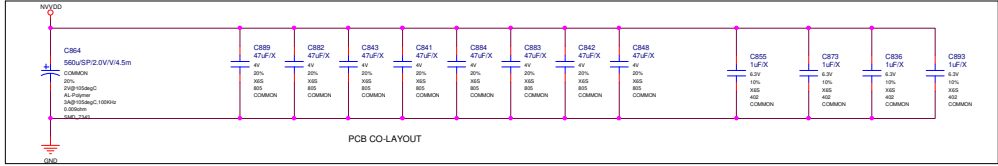
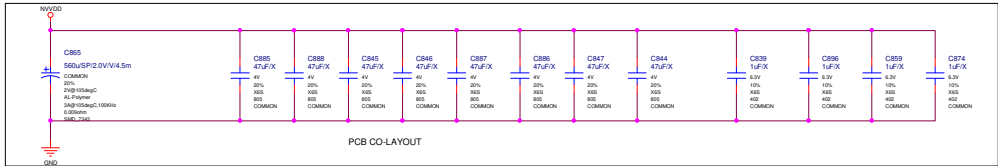




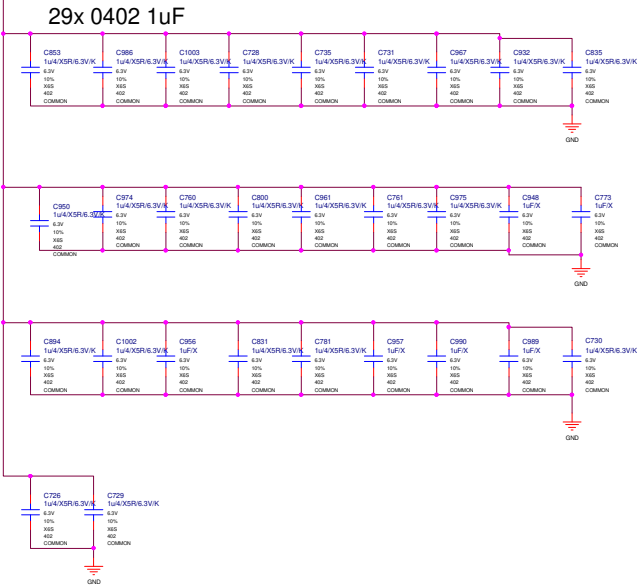
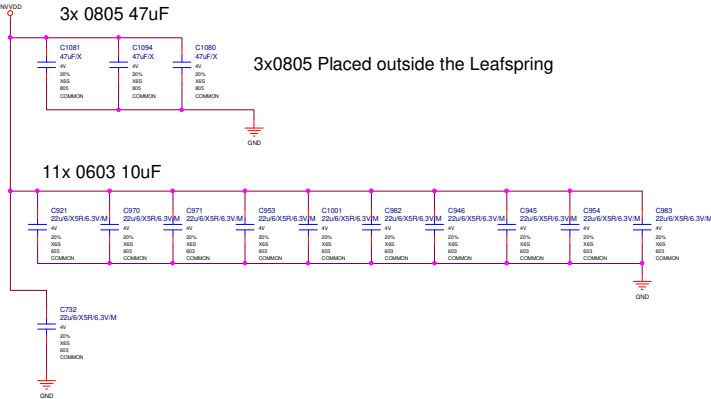
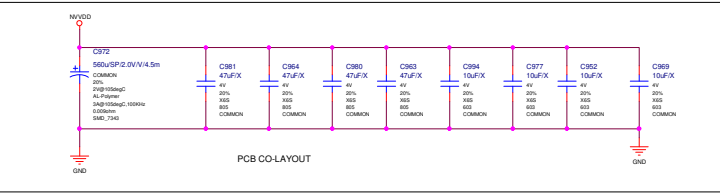


FBVDDQ



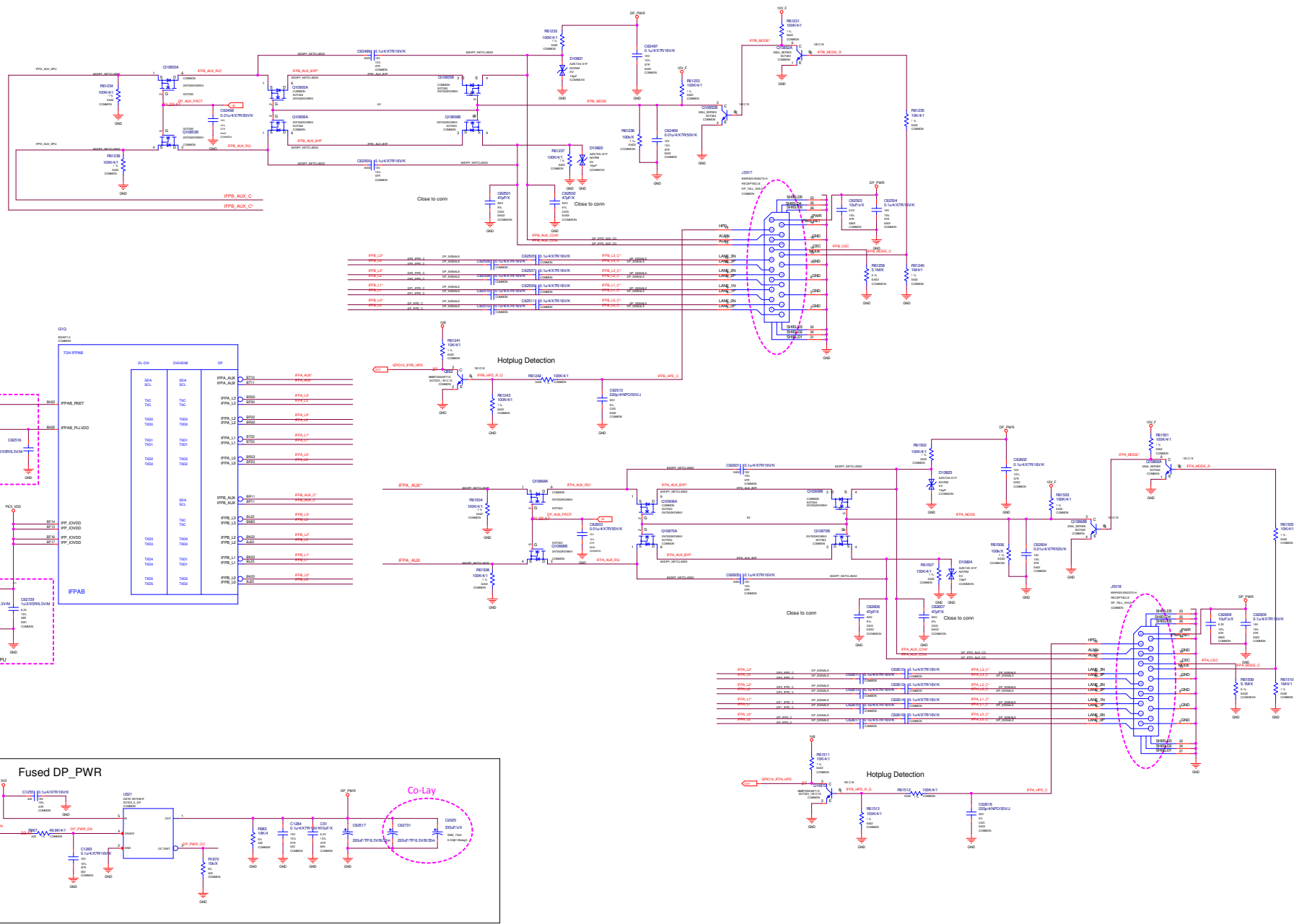


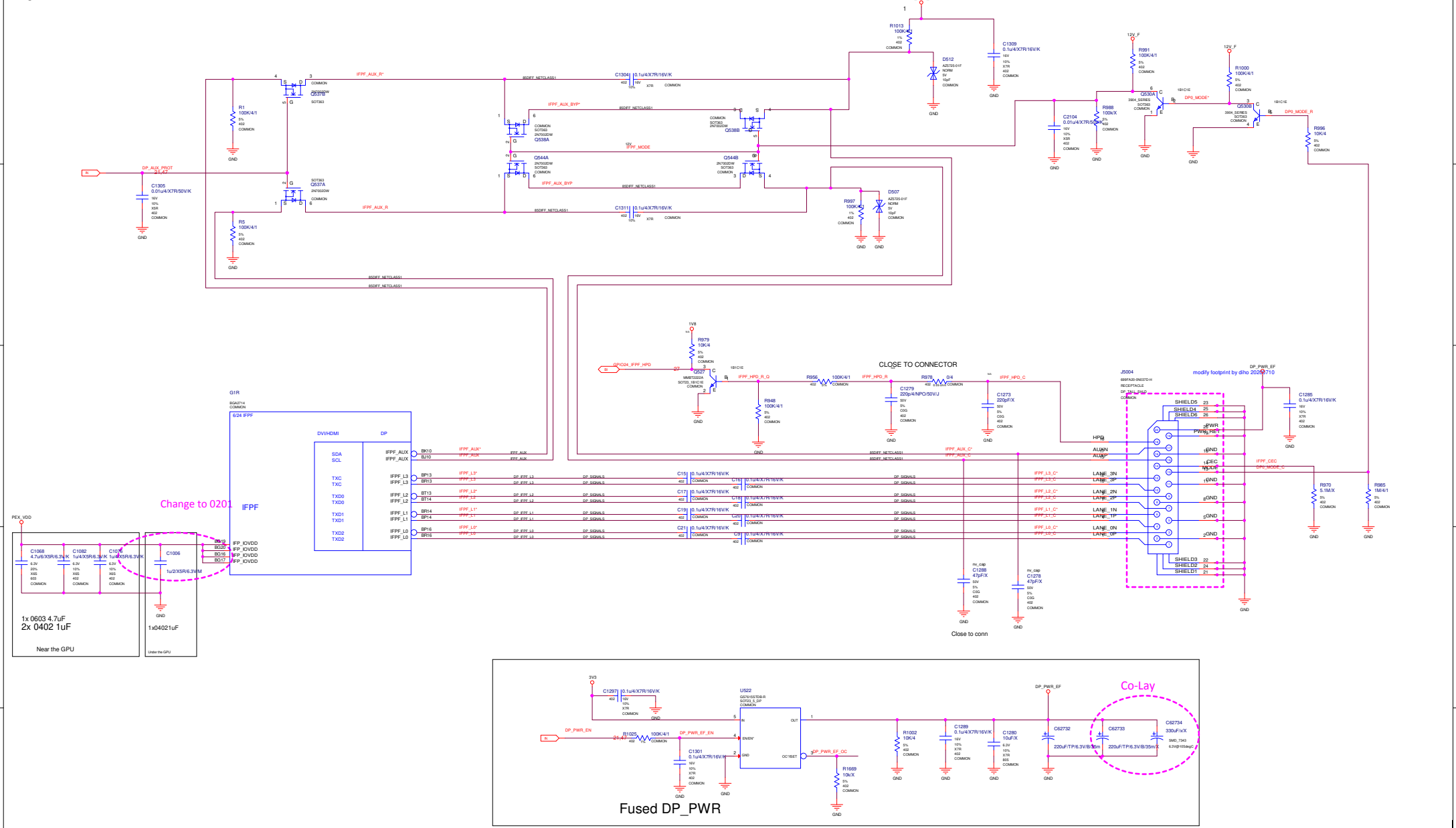
UNDER GPU



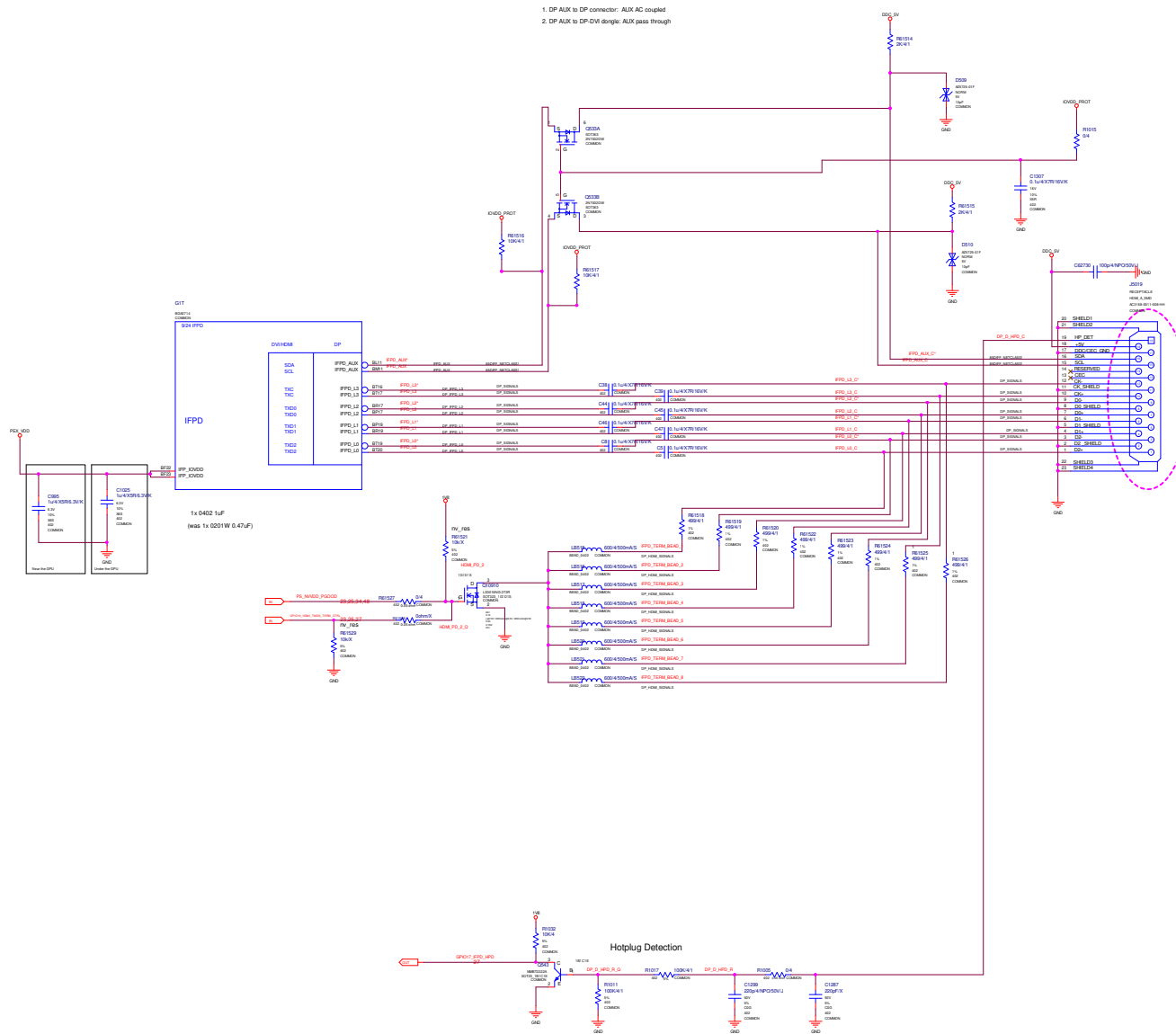
UNDER GPU

## IFPA, IFPB For DP x2

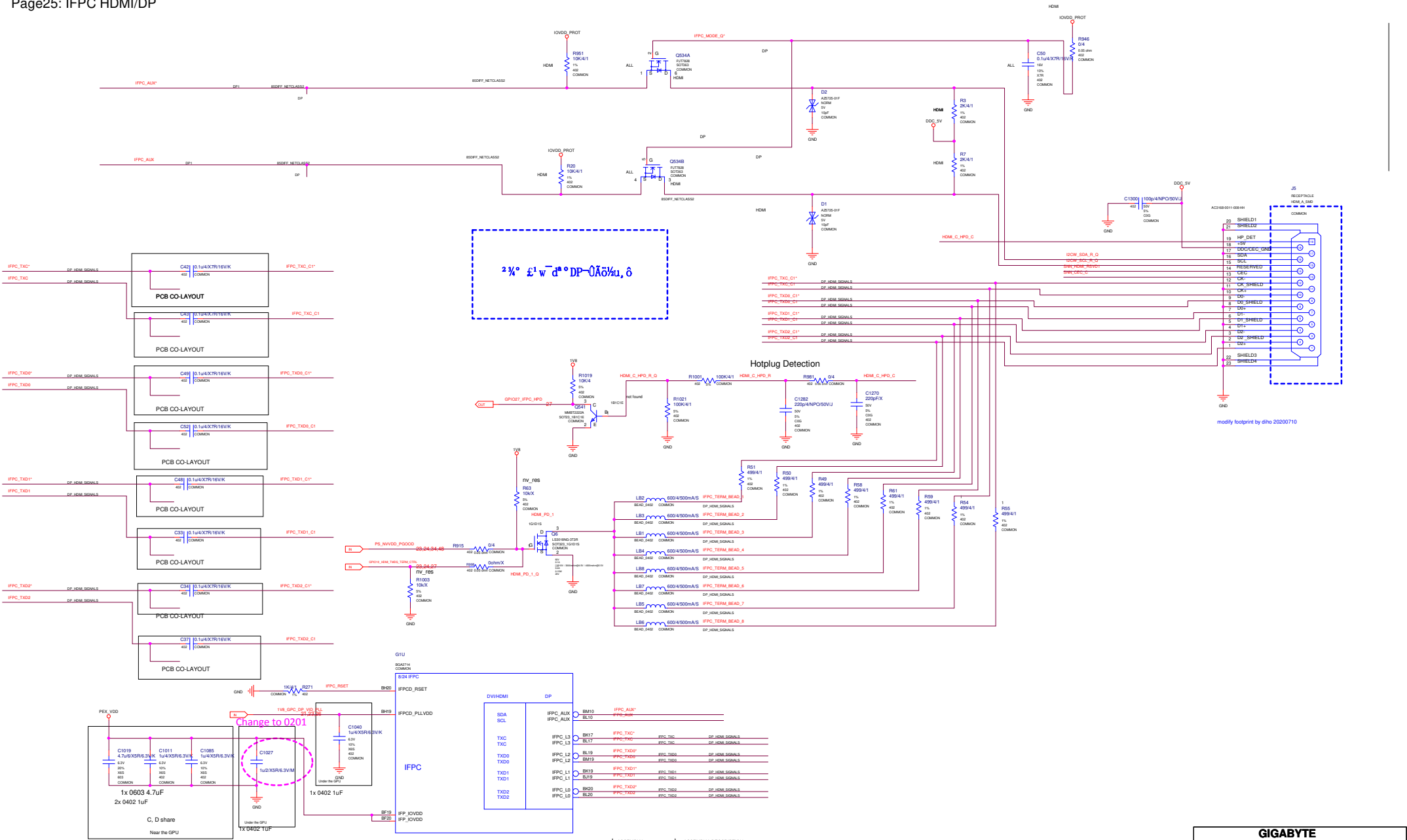












STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
TBD				

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
H	H	M	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

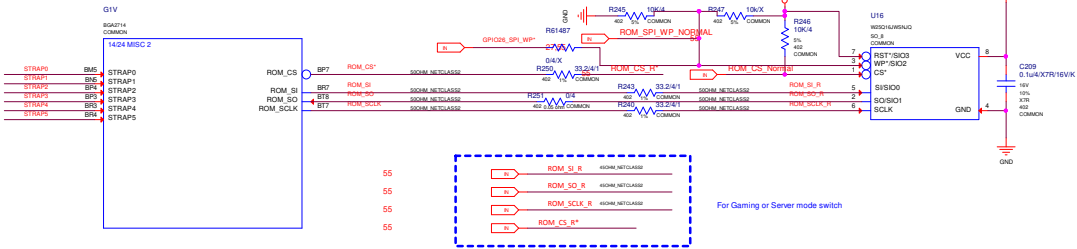
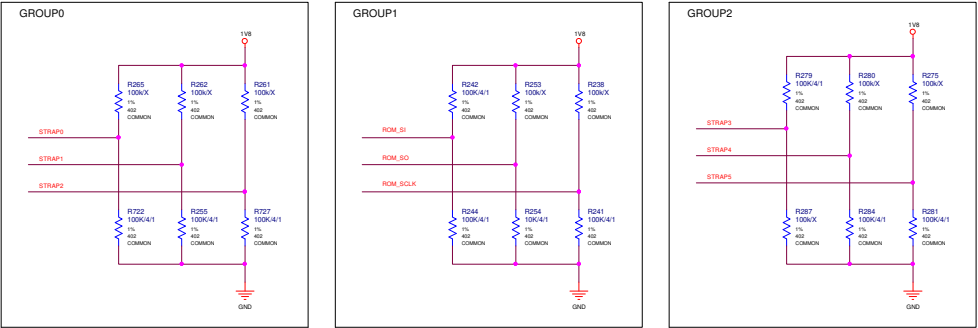
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

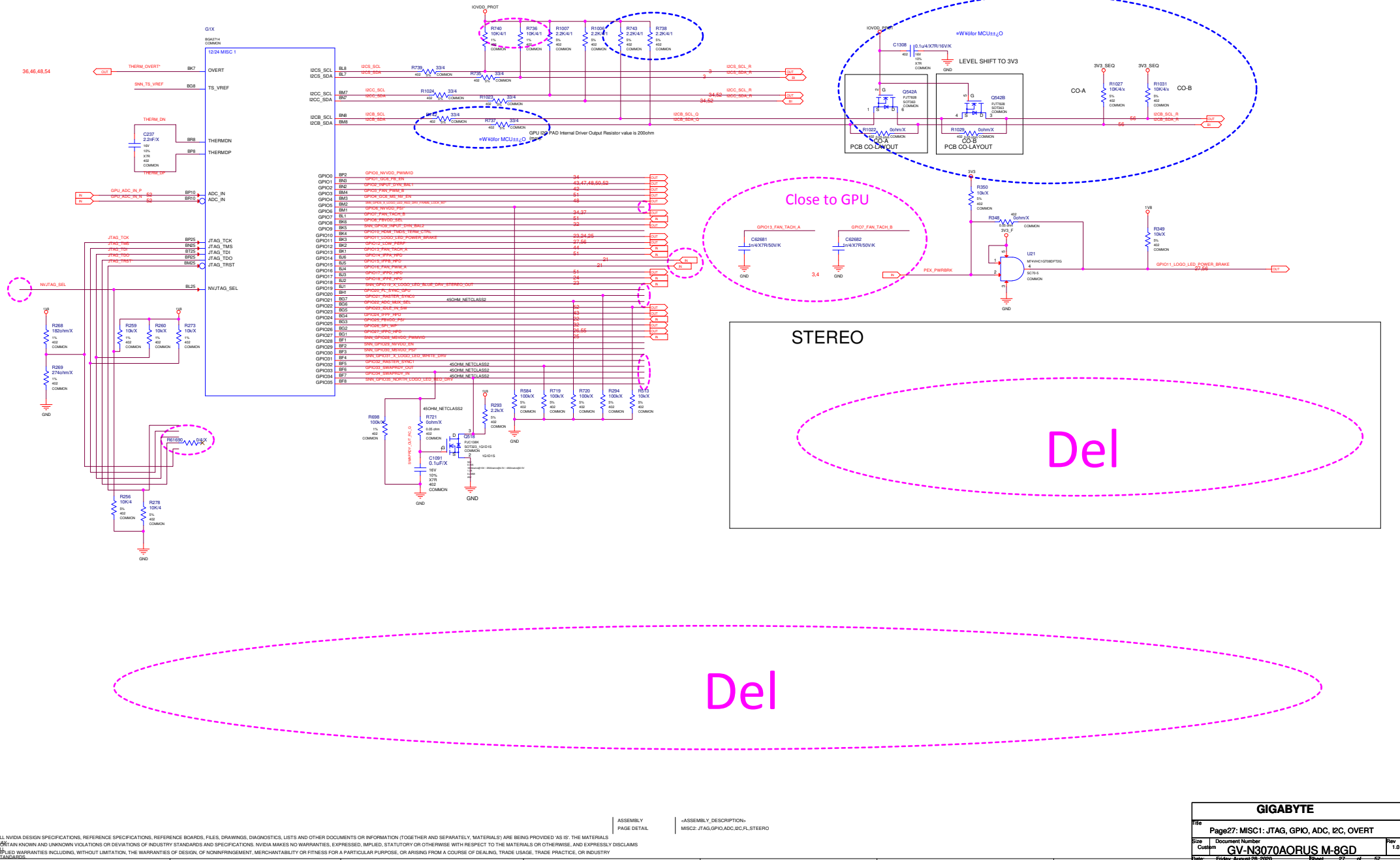
1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE

1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL

1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER

1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE





Del NV LED

WHITE DRIVE

LOGO LED WHITE

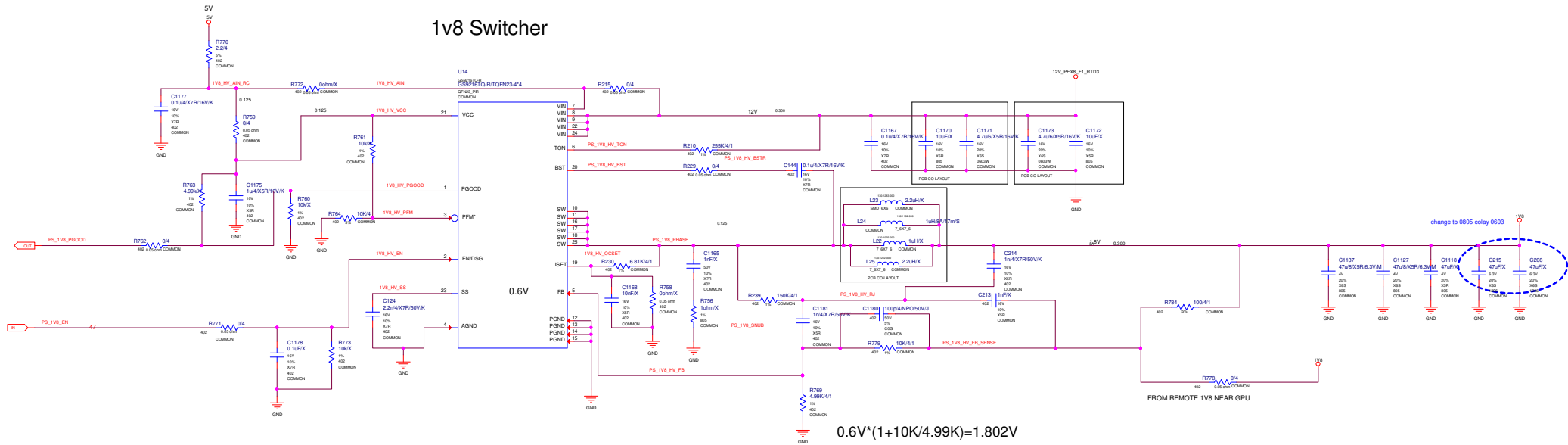
LOGO LED RED

RED DRIVE

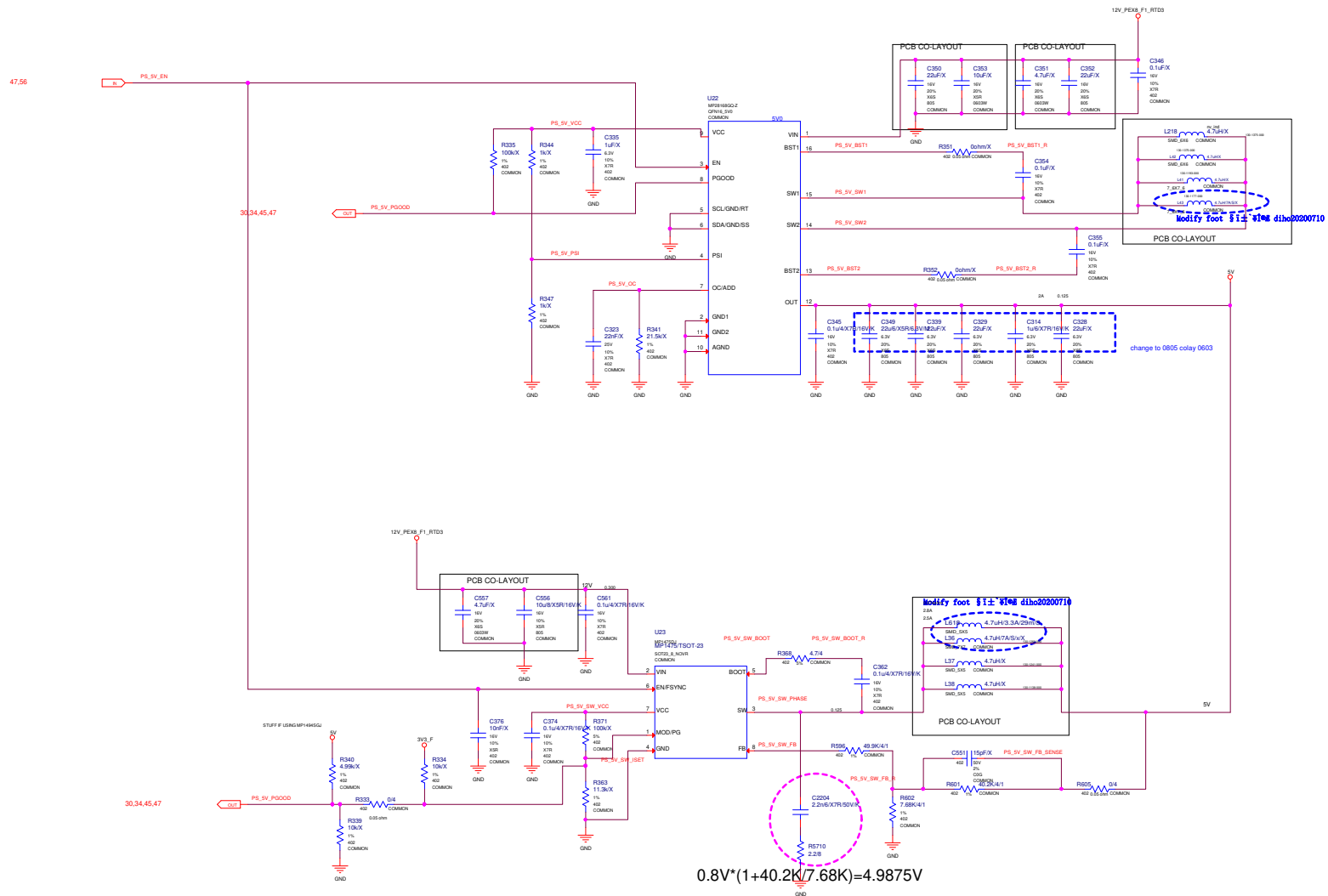
GREEN DRIVE

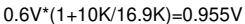
BLUE DRIVE

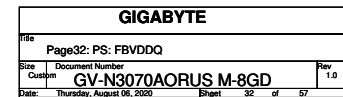
## 1v8 Switcher



$$0.6V \cdot (1 + 10K/4.99K) = 1.802V$$

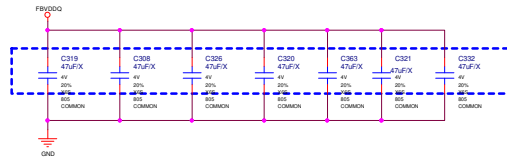
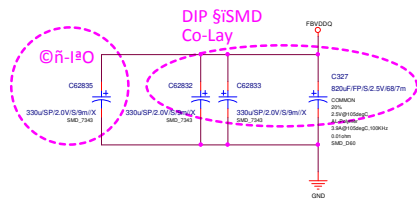
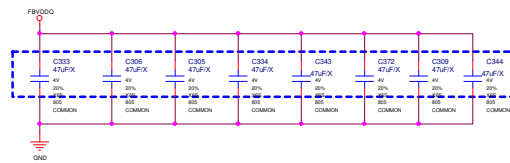
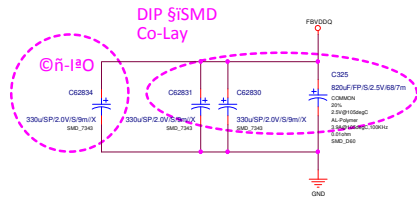
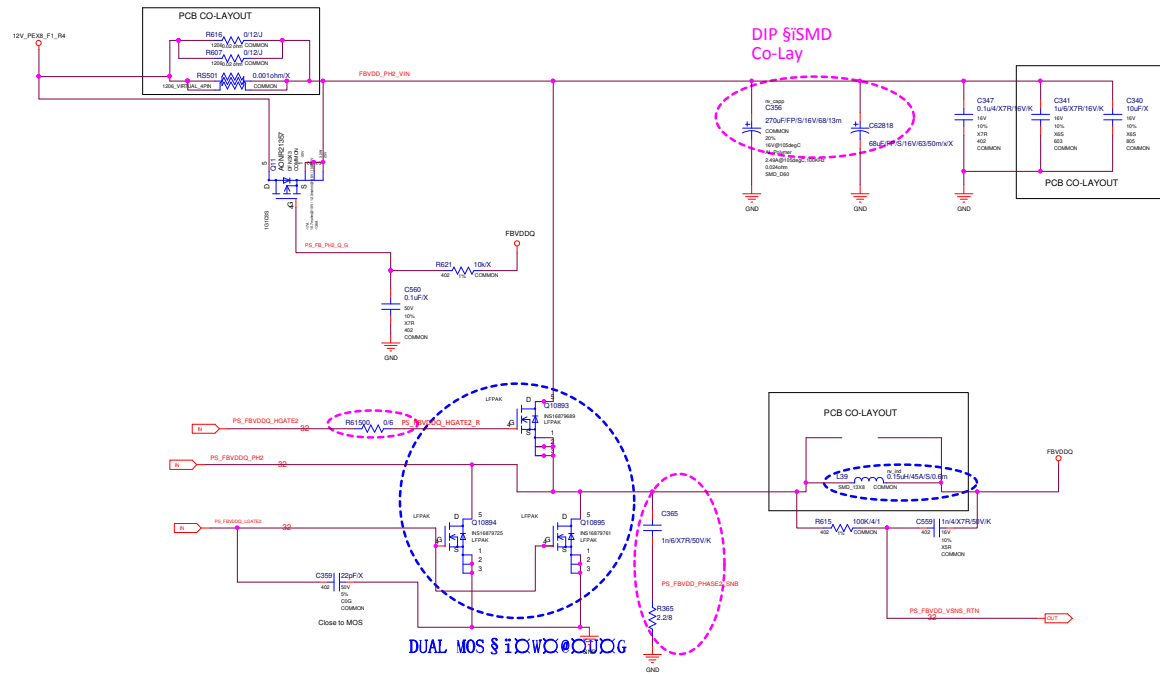


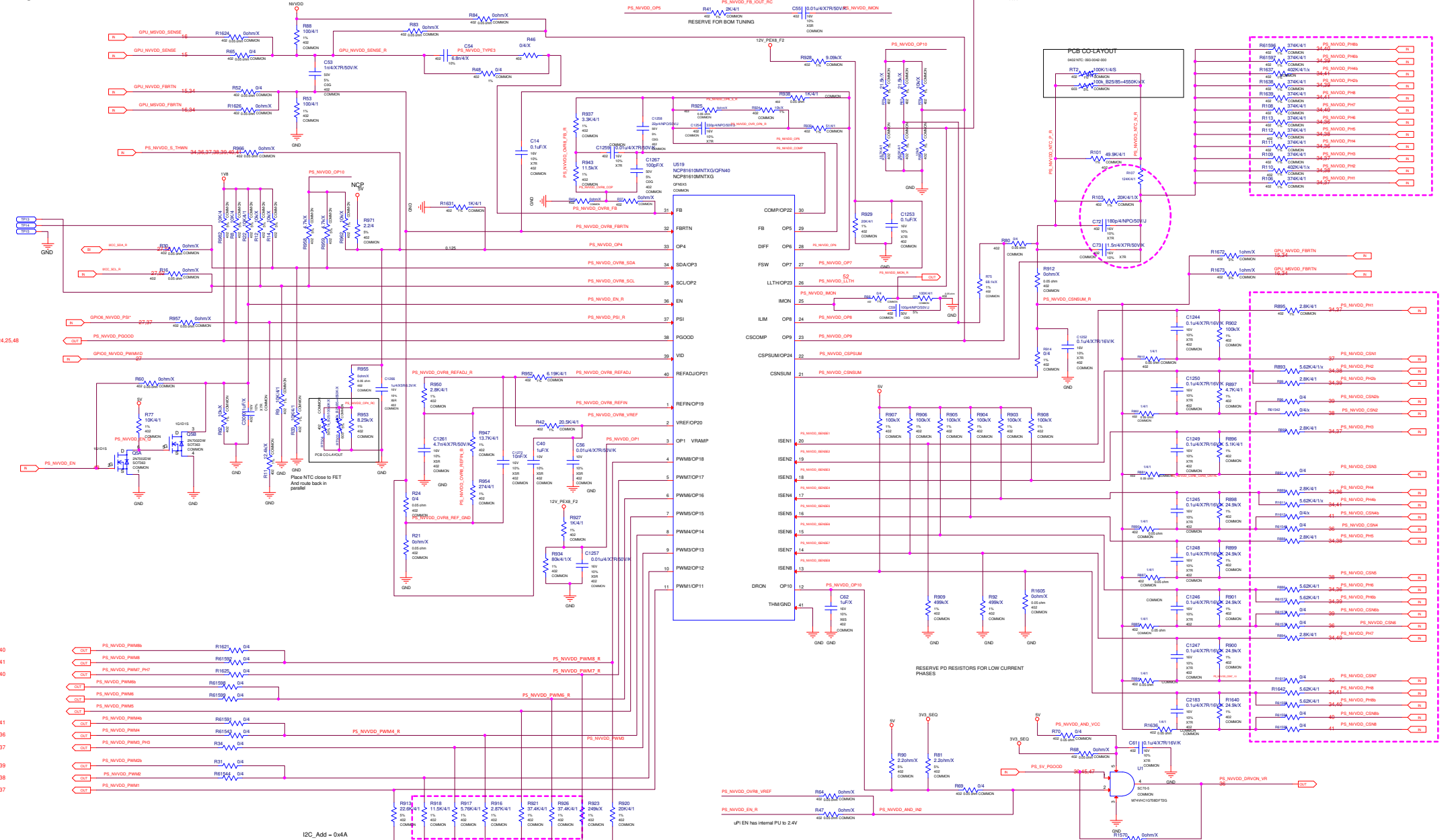






## FBVDD PH2 INPUT ANTI-BACKDRIVE





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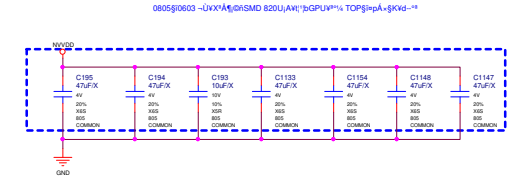
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Size Custom	Document Number GV-N3070AORUS M-8GD		Rev 1.0
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DIP ŞİSMD  
Co-Lay

DIP ŞİSMD  
Co-Lay



Rev	1.0
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**DIP 5SMD Co-Lay**

080509063 ~00xH<sub>2</sub>OxSMD 820U/ANV11111111 TOP/IN4A-400V-11

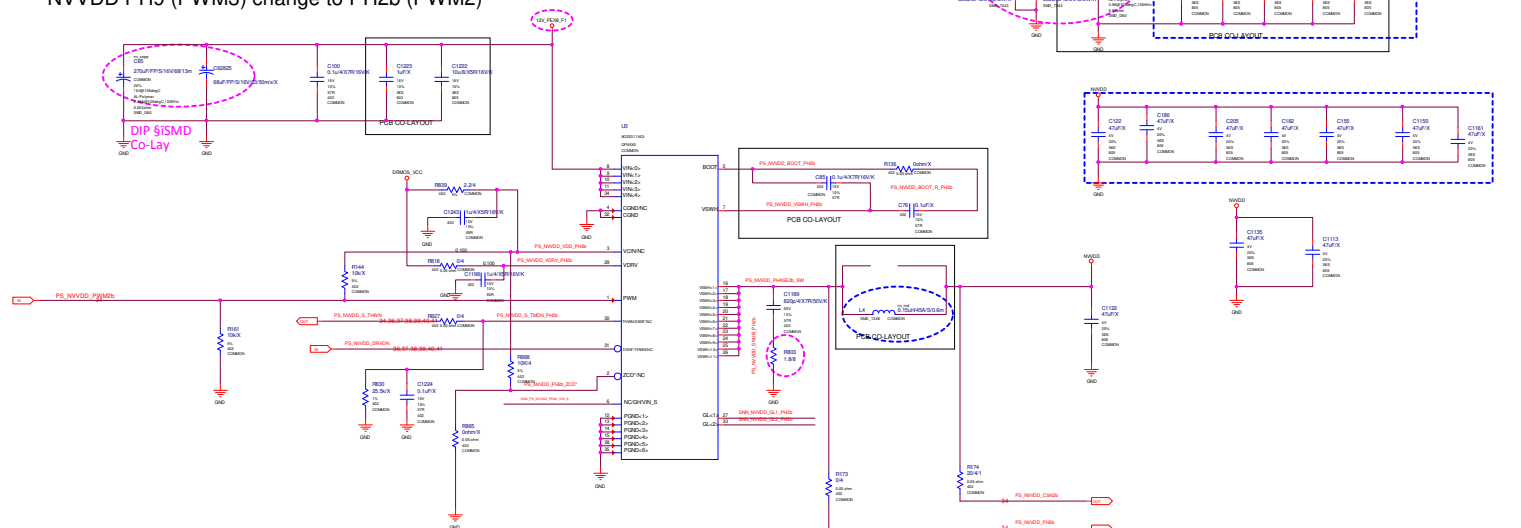
PCB CO-LAYOUT

Diagram illustrating the PCB CO-LAYOUT for the DIP 5SMD Co-Lay component. The layout shows the component connected to the PCB via a series of capacitors (C146, C175, C168, C156, C136, C131) and a common ground connection. The component is labeled with part number 080509063 and specifications ~00xH<sub>2</sub>OxSMD 820U/ANV11111111 TOP/IN4A-400V-11. The PCB layout includes a dashed blue box indicating the component area and a dashed red box indicating the connection area.

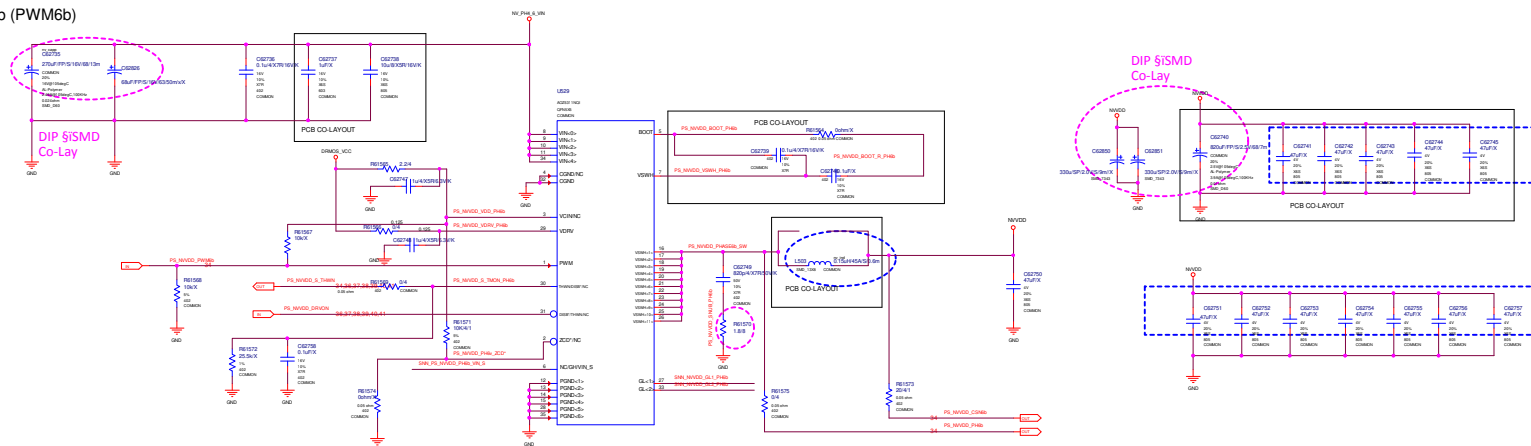
## GIGABYTE



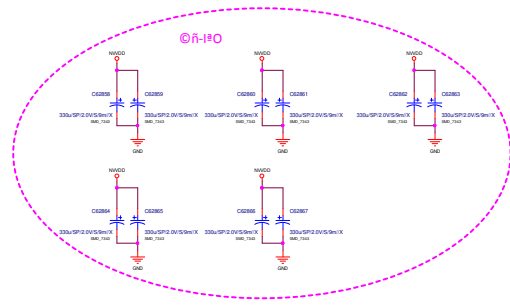
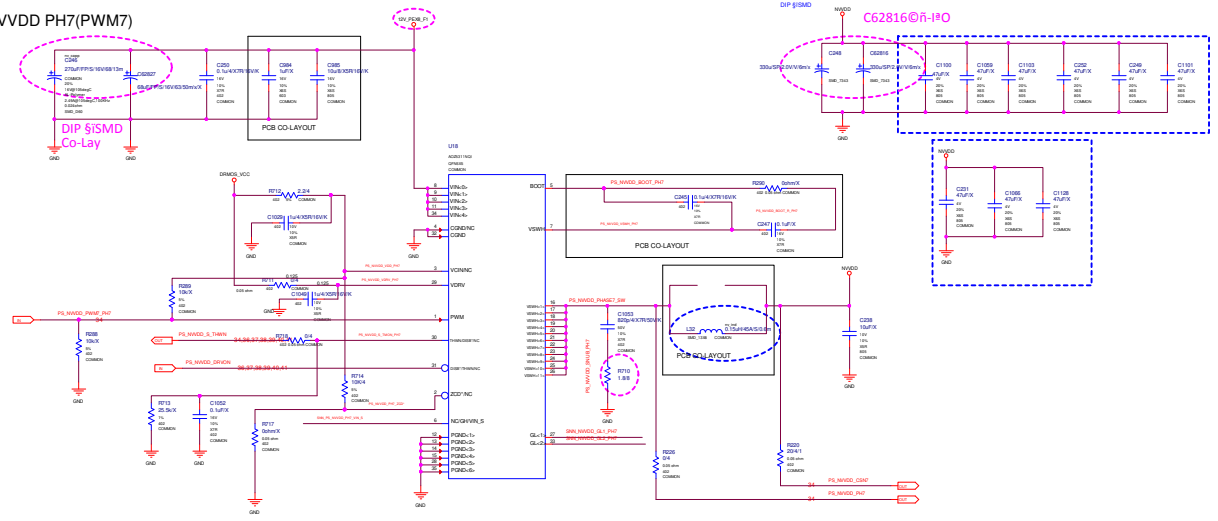
NVVDD PH9 (PWM3) change to PH2b (PWM2)



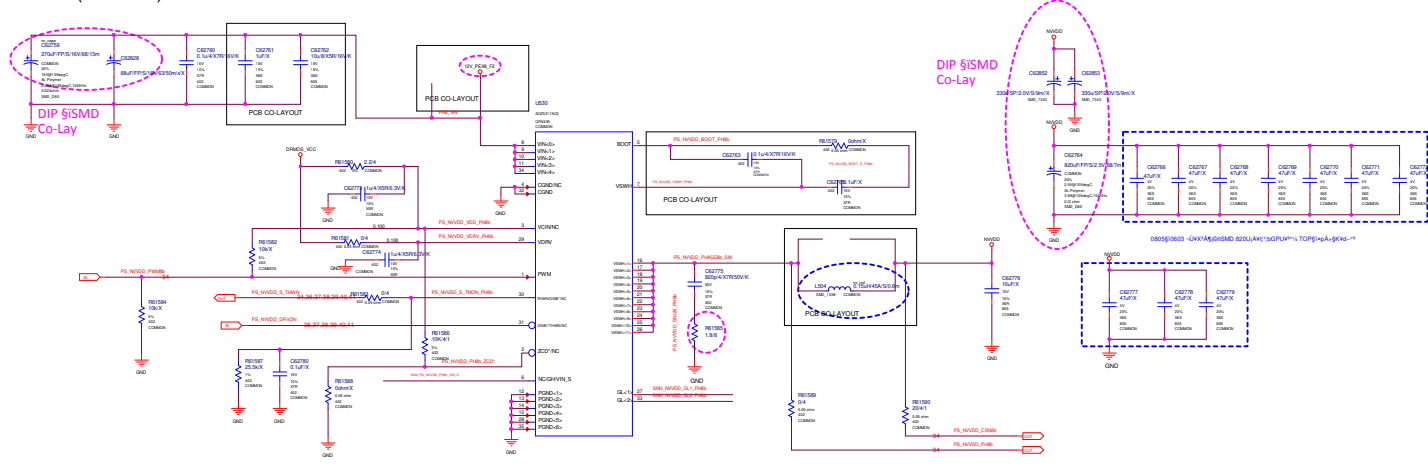
NVVDD PH6b (PWM6b)



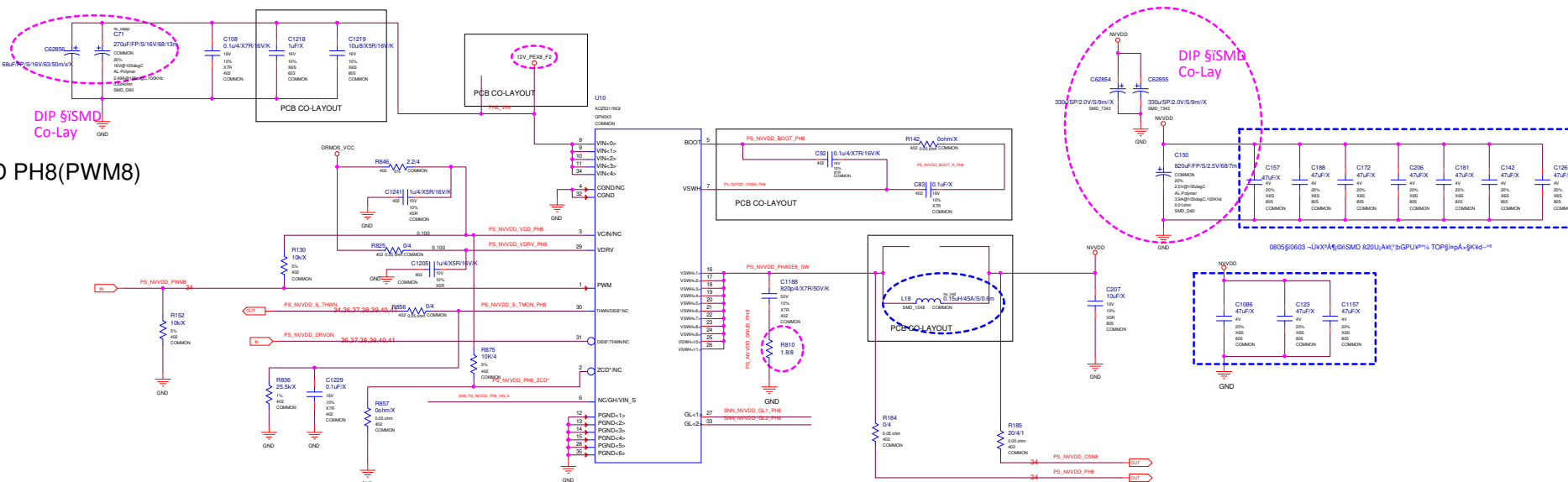
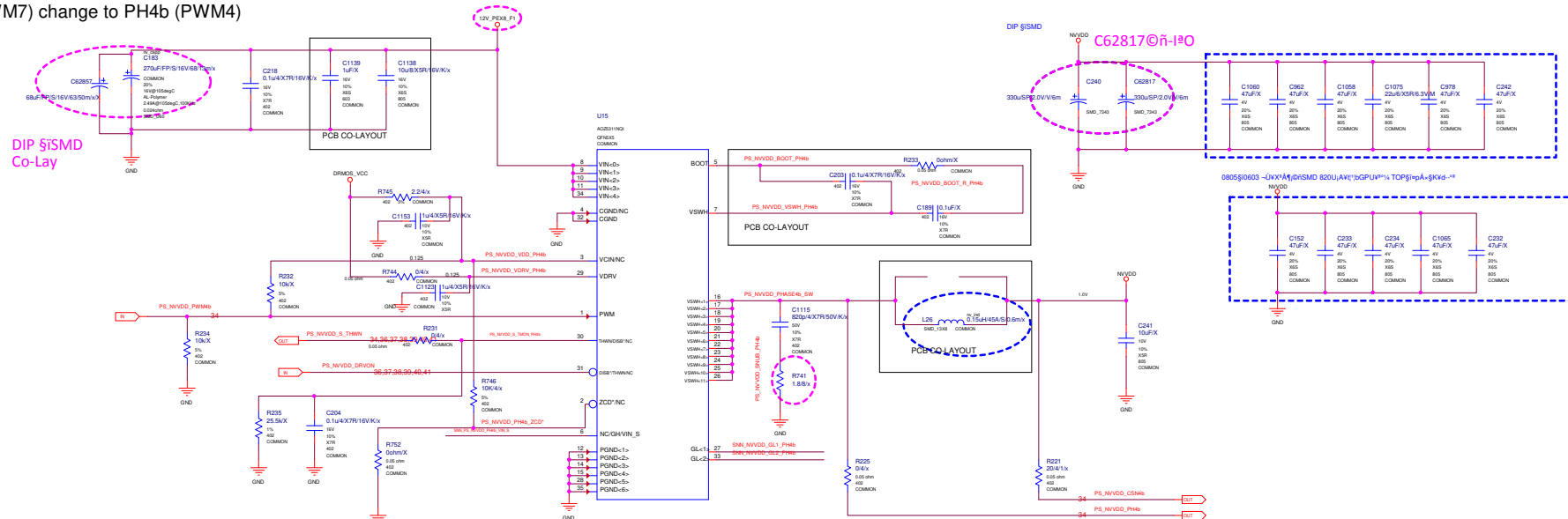
NVVDD PH7(PWM7)

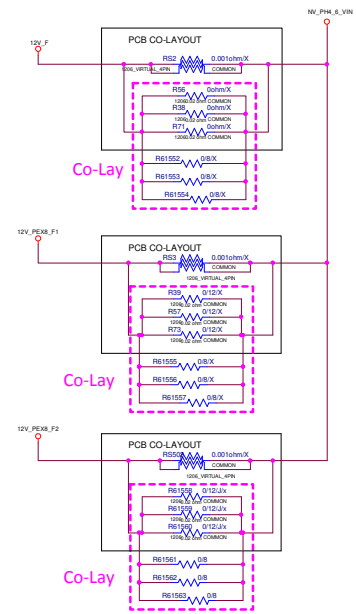
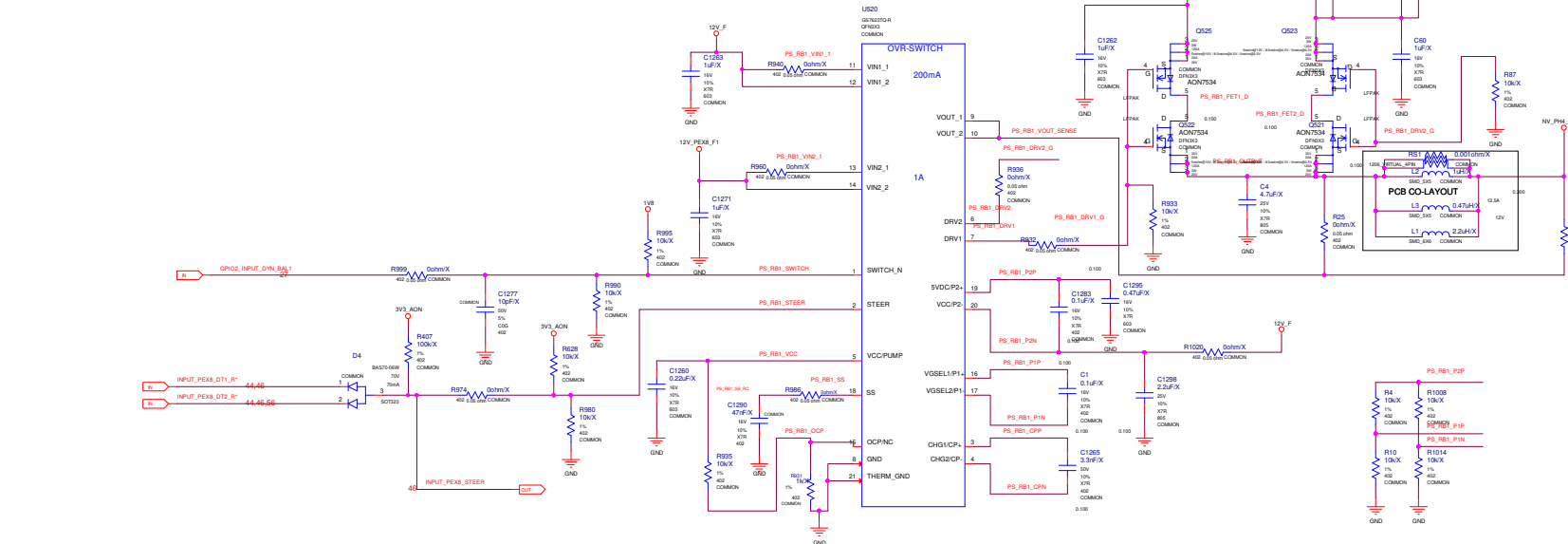


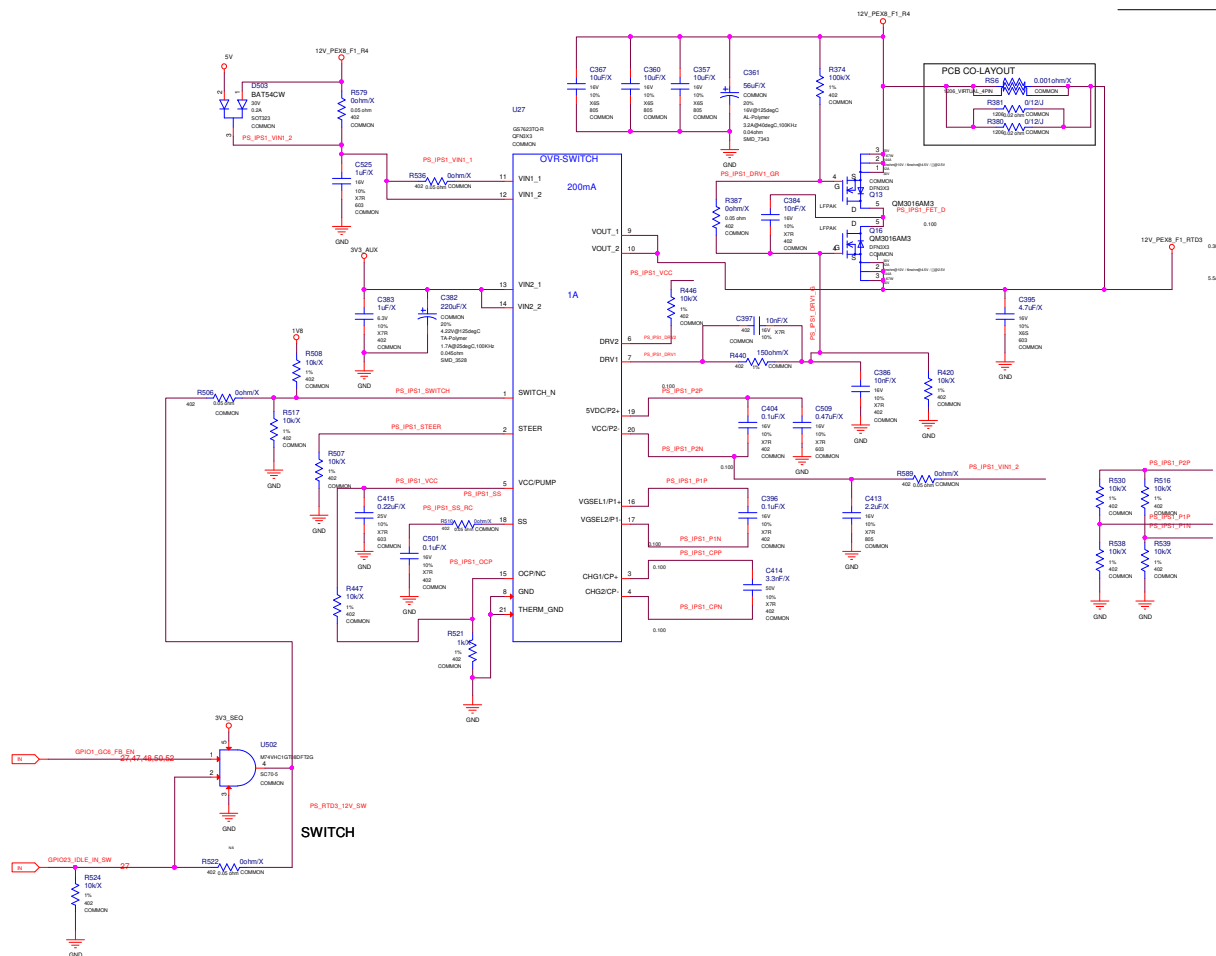
NVVDD PH8b (PWM8b)





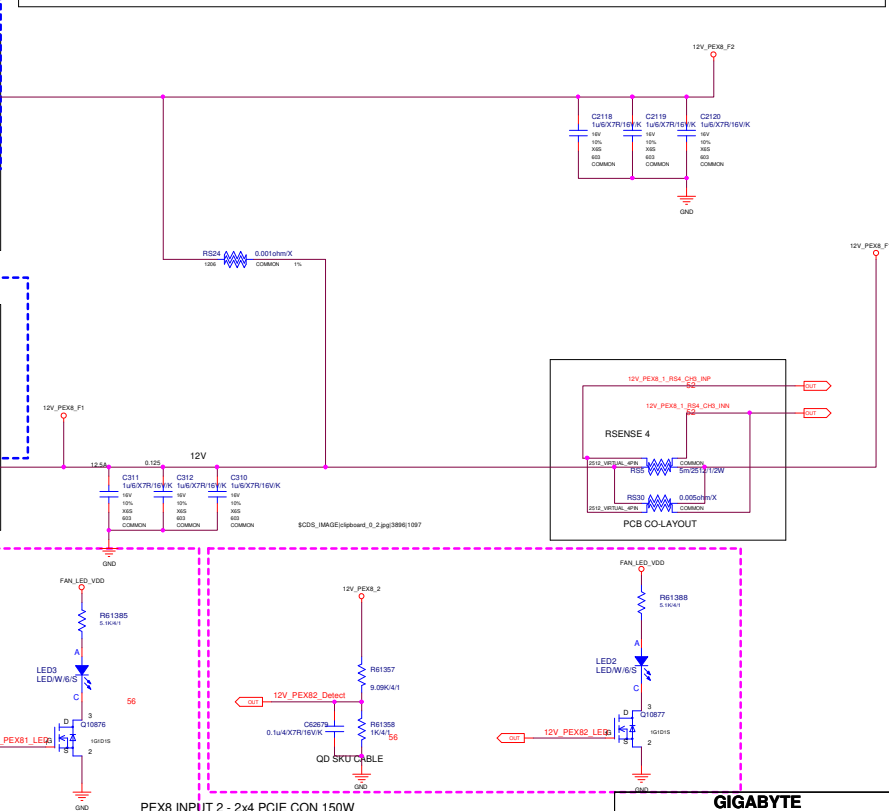
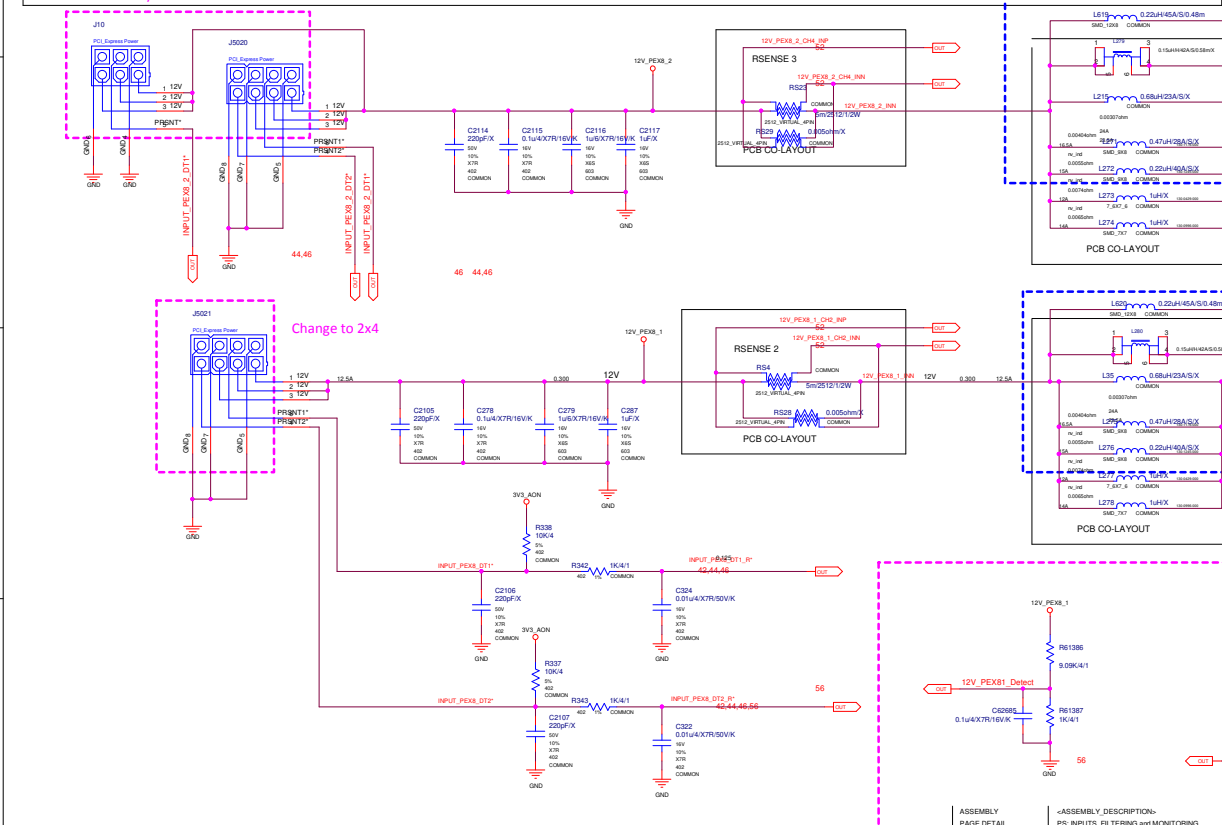


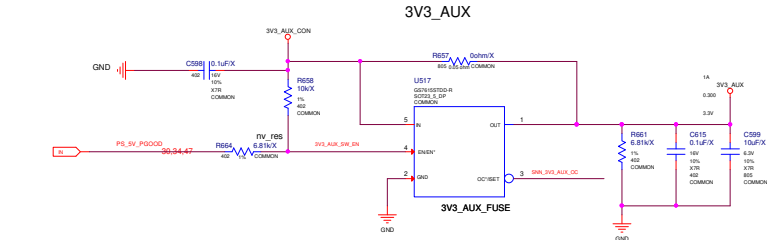
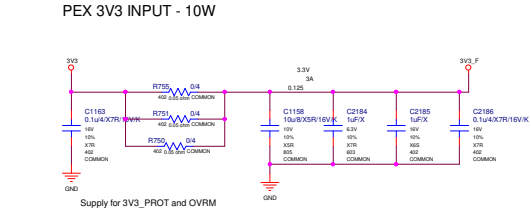
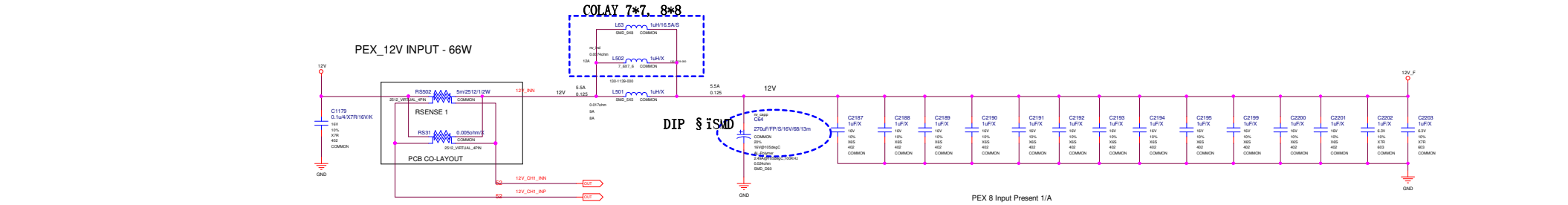




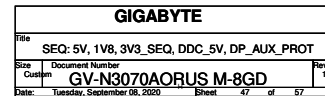
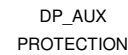
GPI01	GPI029	SWITCH	VOUT
0	0	0	12V
0	1	0	12V
1	0	0	12V
1	1	1	3V3A

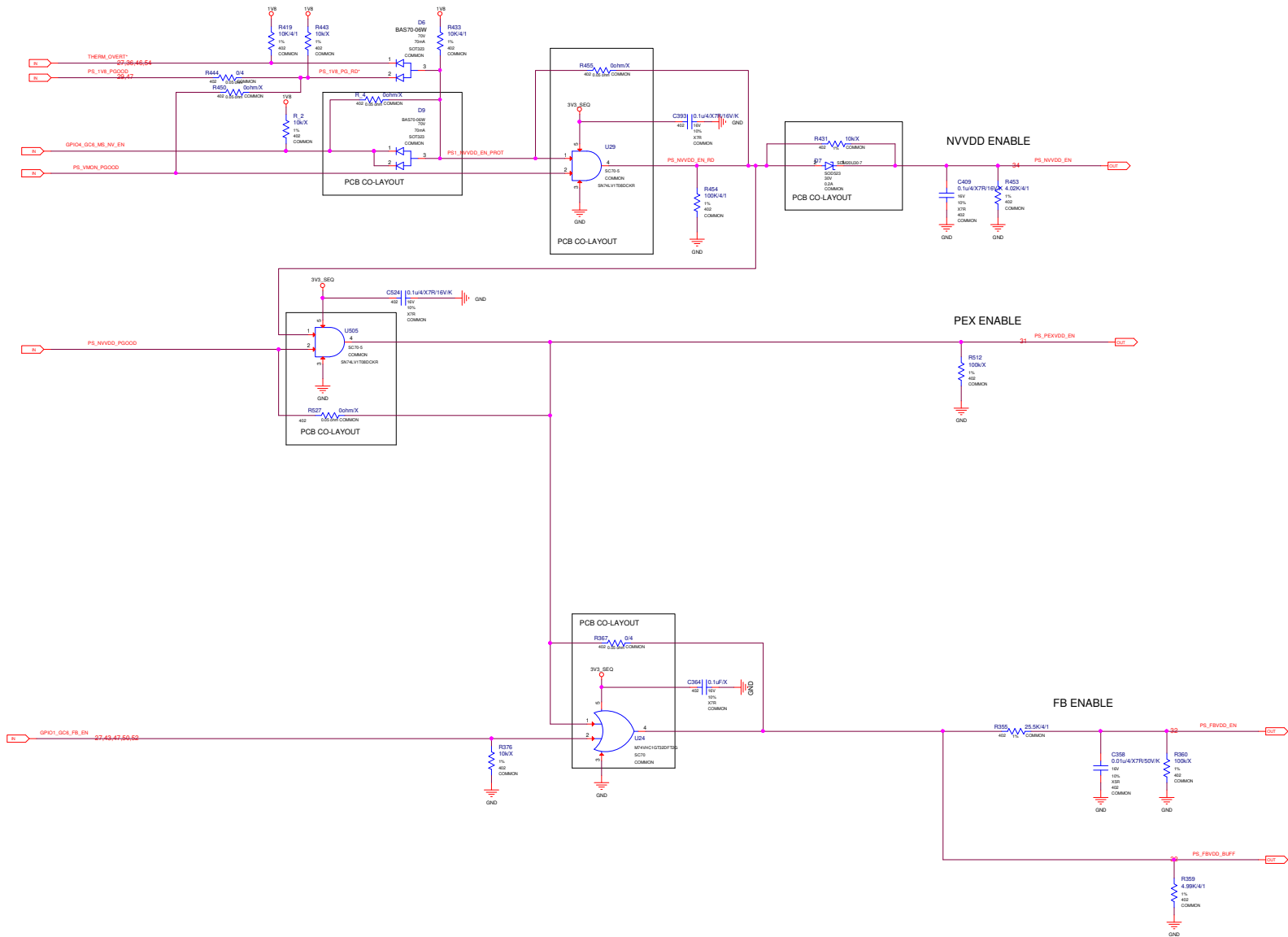
SWITCH	VOUT
0	$V_{OUT} = V_{IN1}$
1	$V_{OUT} = V_{IN2}$



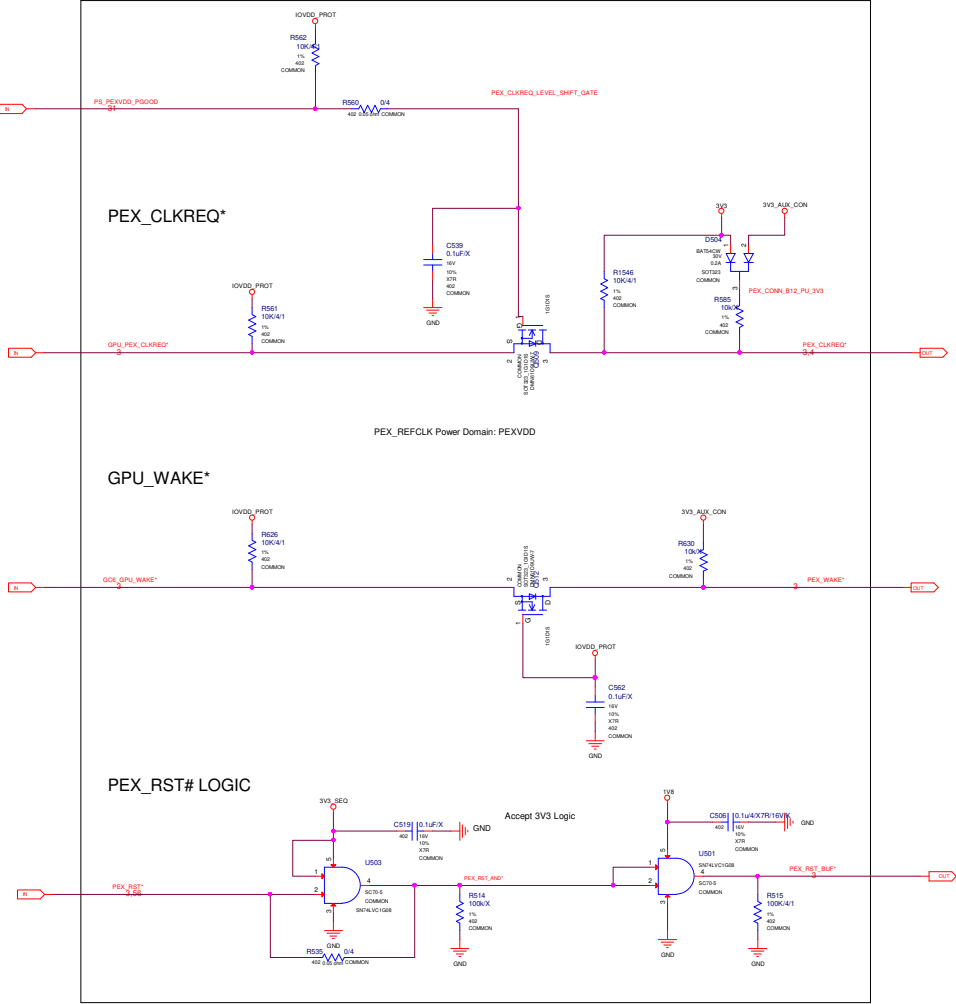










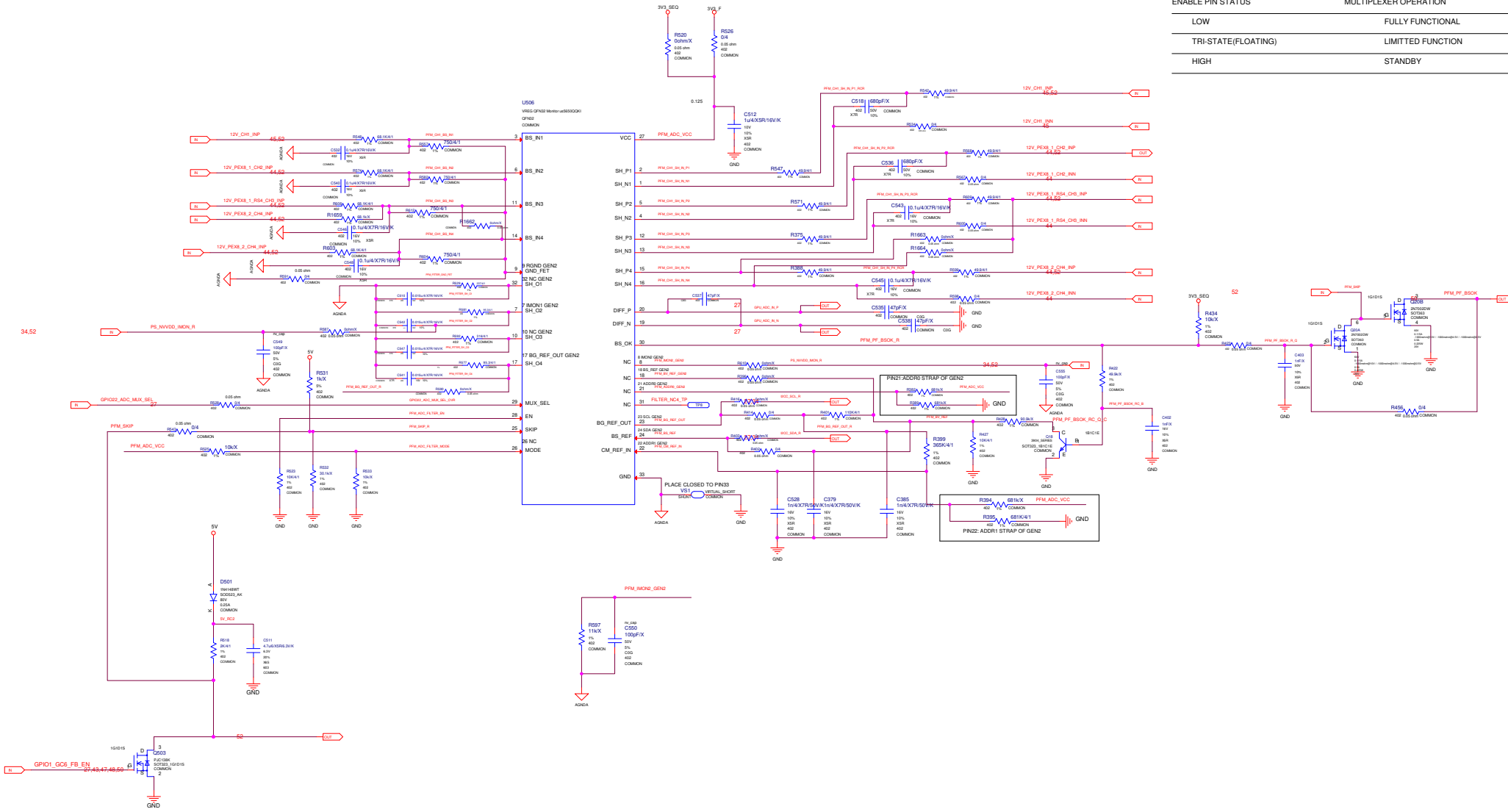




OPTIONS	PEX3V9_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

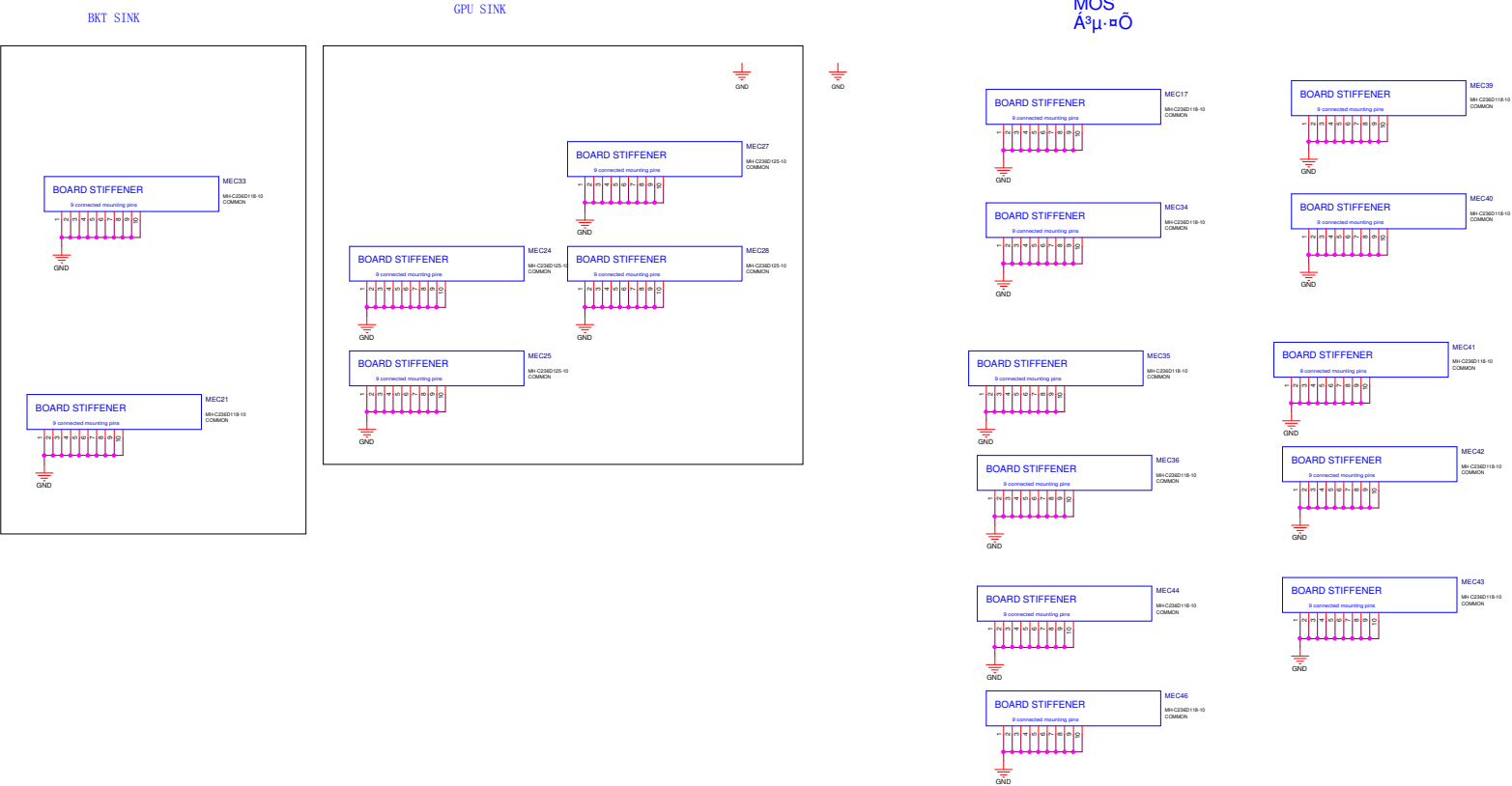
Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
G06_FB_EN	INPUT	Indicator for RTD3/G06s residence, Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221 (VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221 (PV) or Pre-filter(BS_OK)

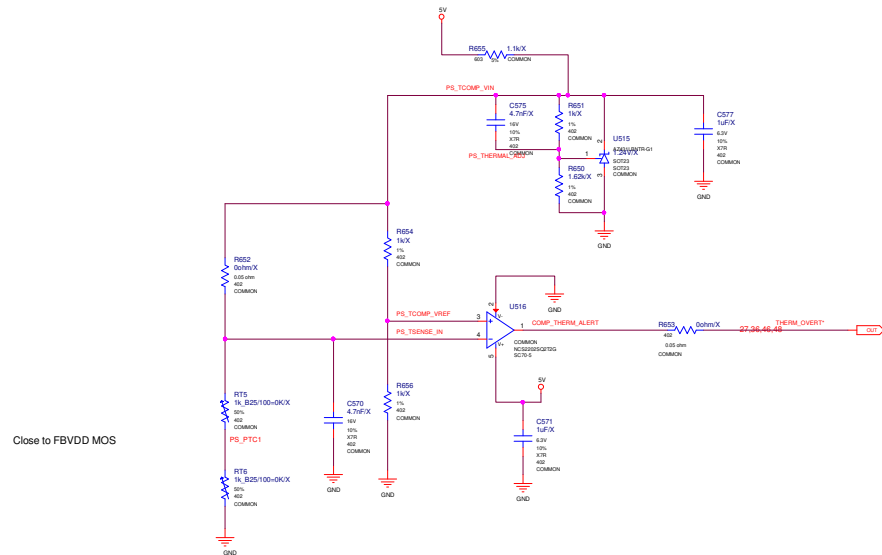




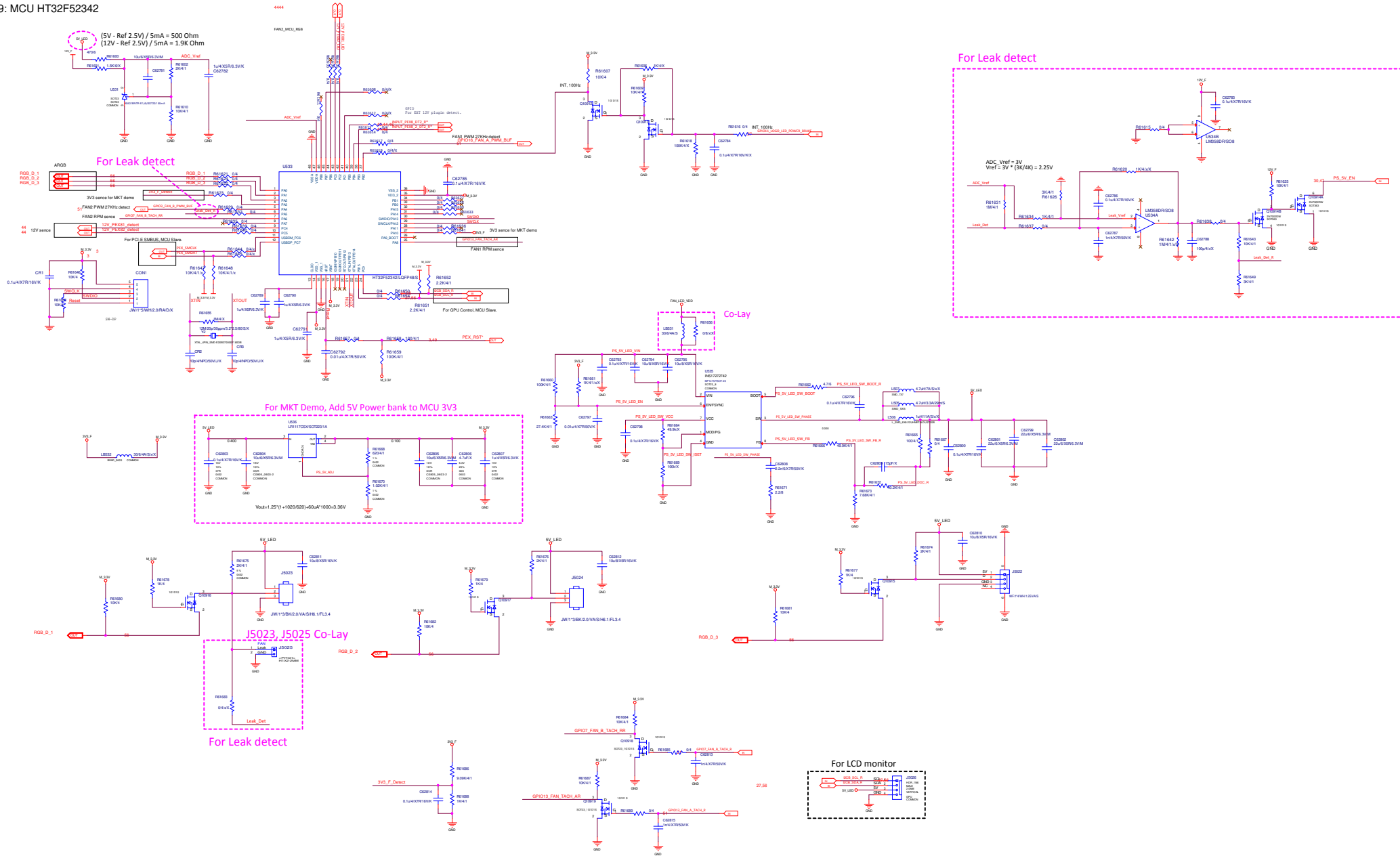
MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

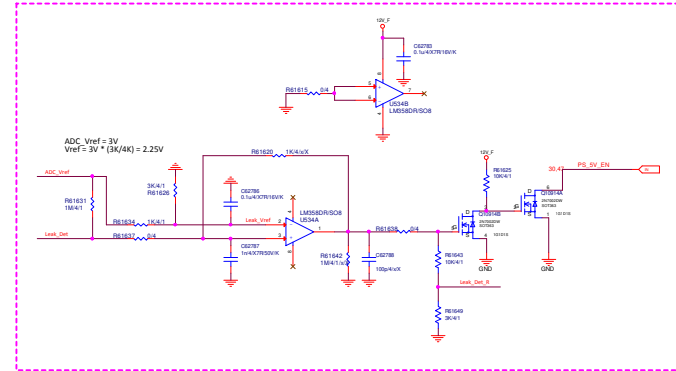




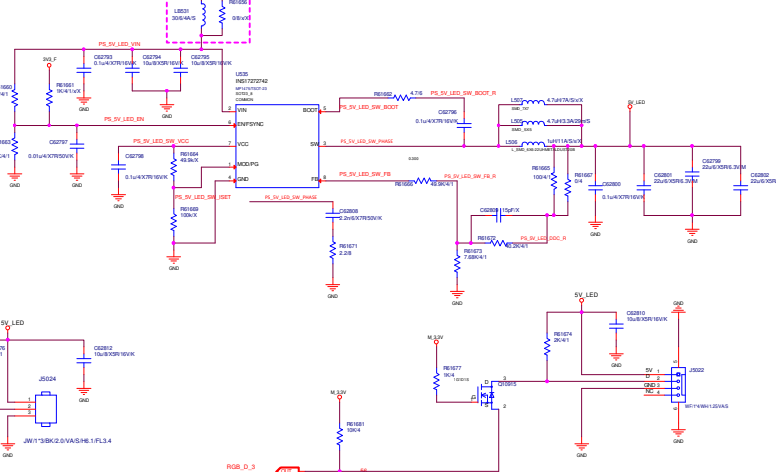




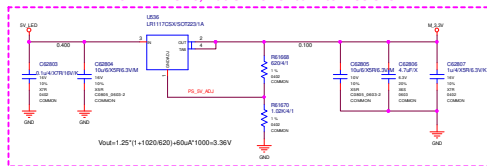
For Leak detect



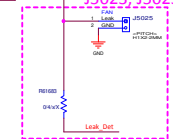
Co-Lay



For MKT Demo, Add 5V Power bank to MCU 3V3

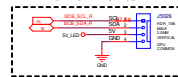


J5023, J5025 Co-Lay



For Leak detect

For LCD monitor





History

Date	Modify
2018.07.21	First version